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Implementation Of Reversible Logic Adder Circuits And Their Power Analysis

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Abstract
In modern VLSI design, the device dimensions are shrinking(scaling) exponentially and the circuit complexity is growing exponentially. Device scaling is limited by the power dissipation, which in turn demand for better power optimization methods. This has led to the development of reversible circuits. The conventional digital circuits designed using basic logic gates AND, OR, EX-OR, NAND and NOR are not reversible. This work presents a literature survey on reversible circuits. Then few existing reversible gates like Feynman, Tofolli, Fredkin, Peres are implemented using Xilinx 12.3 tool. Subsequently half adder and full adder circuits are implemented using these gates. This work focuses on measuring the power consumption of all the implemented reversible circuits using Cadence Encounter RTL compiler tool.

Keyword-Reversible logic, Feynman, Tofolli, Fredkin, Peres, Power consumption

I. INTRODUCTION

The main requirement in VLSI design, particularly in portable device technologies with increasingly high computation requirements, power consumption is an important issue. Power optimization can be done at various abstraction levels in CMOS VLSI design such as Device (Technology) level, Circuit level, Logic level, Architecture (System) level and Algorithmic level. One such method at circuit logic level is energy recovery method, which employs reversible logic gates [7]. The computation carried out in conventional computers is irreversible, such as once a logic block generates the output bits, the input bits are lost. This loss of input bits leads to the power consumption in the system. Landauer has shown that for every bit of information lost in logic computations that are not reversible, kT∗ log2 joules of heat energy is generated, where k is the Boltzmann's constant, and T is the absolute temperature at which the computation is performed[1]. The energy dissipation due to bit loss is not significant for the current clock speed of computers. However, as the clock speeds of computers are elevated, the frequency with which the information bits are lost will also increase[5]. If logic gates are designed such that the information bits are not destroyed, the power consumption can be reduced dramatically. The information bits are not lost in case of a reversible computation. Bennett showed that a zero power dissipation in logic circuits is possible only if a circuit is composed of reversible logic gates. The Reversible Computing Research Group, Massachusetts Institute of Technology, has developed a proof-of-concept reconfigurable reversible chip, which is called the FlatTop[6].Reversible logic is becoming more and more prominent optimization technique having its applications in low power CMOS designs, Quantum computing, Nanotechnology and Optical Computing.

II. REVERSIBLE LOGIC GATES

A reversible gate is a logical cell that has the same number of inputs and outputs with a bijective mapping between the input and output vectors. Thus, inputs of a reversible gate can be uniquely determined from its outputs. A reversible gate with *n*-inputs and *n*-outputs is called a *n x n* reversible gate. In an *n*-output reversible gate, the output vectors are permutations of the numbers 0 to $(2^n - 1)$. There are several synthesis techniques to design reversible gates. An important metric for evaluating reversible circuits is the Garbage count. Garbage is defined as the number of outputs added to make an n-input k-output Boolean function (*(n, k)* function) reversible. Some of the major problems with reversible-logic synthesis are [5]:

1) Fanouts are not allowed.
2) Feedback from gate outputs to inputs is not permitted.

Recently, researchers illustrated that feedback is allowed in reversible computing while designing the sequential [9].
A logic synthesis technique using a reversible gate should have the following features :

1) use a minimum number of garbage outputs
2) use a minimum input constants
3) use a minimum circuit level
4) use a minimum number of gates

An elaborate list of reversible gates studied in the literature is presented in [4]. Some prominent gates among them are the Feynman gate, the Toffoli Gate, the Fredkin gate and the Peres gate.

A. Feynman Gate

Feynman gate[3] is a 2*2 one-through reversible gate shown in Fig. 1. One-through gate means that one input variable is also the output.

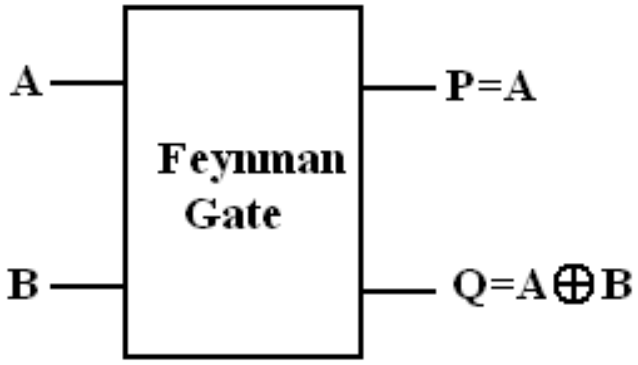

Fig.1. Feynman Gate

The forward and backward computation[8] of the Feynman gate is as follows.
Forward computation

P=A;

If A=0 then Q=B
Else Q=B'

Reverse computation

A=P;

If P=0 then B=Q
Else B=Q'.

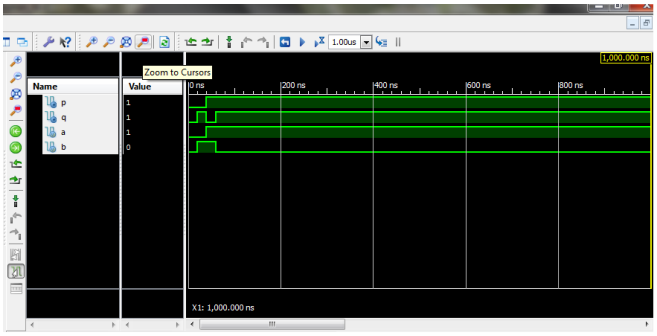

Fig.2. Simulation output of a Feynman Gate

The functionality of the Feynman gate is verified by simulating the Verilog HDL code using Xilinx 12.3 tool. The simulated output is shown in Fig.2.

B. Toffoli Gate

Toffoli Gate (TG) [3]is a 3*3 two-through reversible gate as shown in Fig. 3. Here the outputs P and Q are directly generated from inputs A and B respectively and R = AB⊕C. The forward and backward computations[8] are as follows and the simulated output shown in Fig.4.

Forward Computation:

P=A ; Q=B;

If A AND B =0 then R=C else R=C'

Backward Computation:

A=P ; B=Q;

If P AND Q =0 then C=R else C=R'.

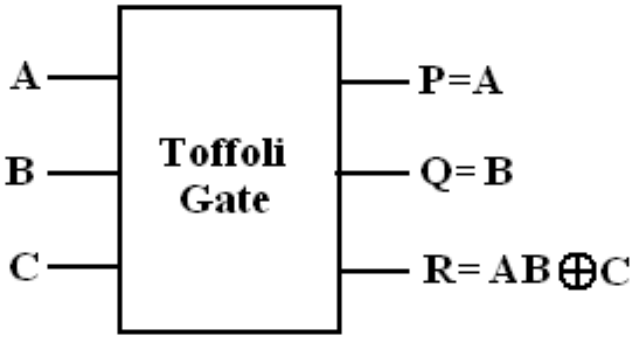

Fig.3. Toffoli Gate

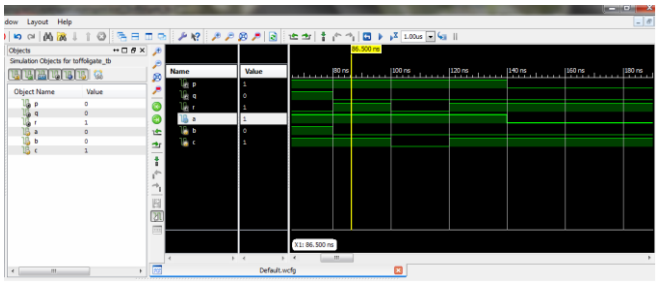

Fig.4. Simulation output of a Toffoli Gate

C. Fredkin Gate

Fredkin gate[4] is a 3*3 conservative reversible gate as shown in Fig.5. It has three inputs

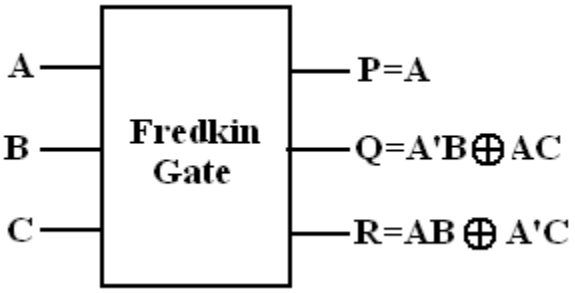

Fig.5.Fredkin Gate

and three outputs. The forward and backward computations for Fredkin gate [8] are explained below and the simulated output is shown in Fig.6.

Forward Computation:

P=A

If A=0 then Q=B and R=C,
else Q=C and R=B.

Reverse Computation:

A=P

If P=0 then B=Q and C=R
else C=Q and B=R

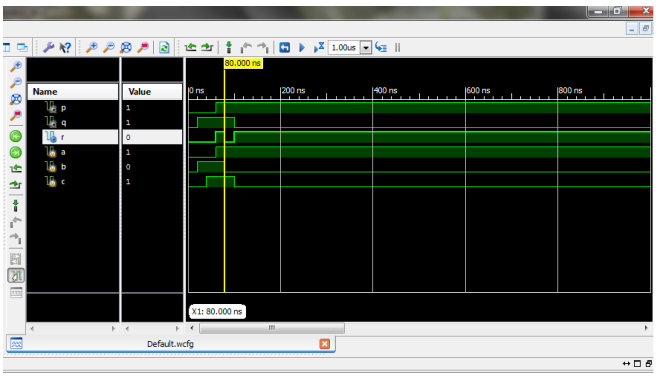

Fig.6. Simulation output of a Fredkin gate

D. ***Peres Gate***

Fig.7 shows a schematic diagram of a Peres gate which is another 3*3 gate having inputs (A, B, C) and outputs P = A, Q = A⊕B, R = AB⊕C. The simulation output of a Peres gate is shown in Fig.8.

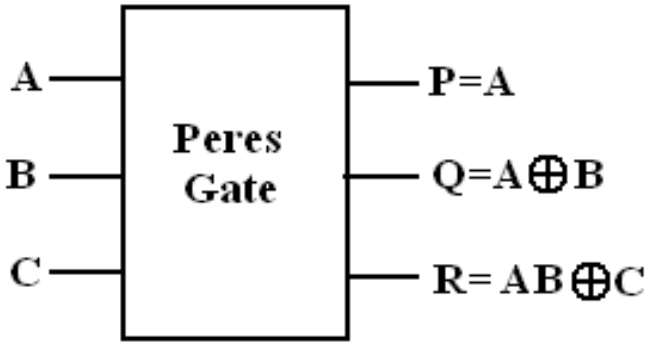

Fig.7.Peres Gate

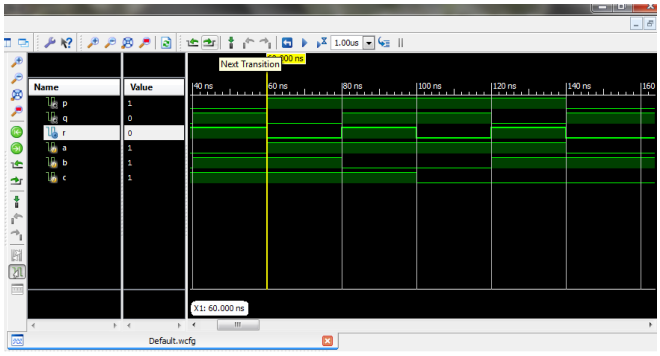

Fig.8. Simulation output of a Peres Gate

E. ***IG Gate***

A 4 * 4 reversible gate having inputs (A, B, C, D) and outputs P = A, Q = A⊕B, R = AB⊕C and S=BD⊕B (A⊕D). The schematic diagram of an IG gate[4] is shown in Fig.9.

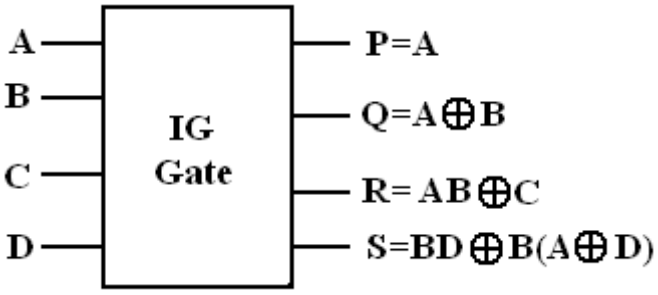

Fig.9. IG Gate

III. REVERSIBLE LOGIC COMBINATIONAL CIRCUITS

Several reversible-logic combinational logic circuits like adders, comparators and ALU are designed and discussed in the literature [2], [3], [7]. This work focuses on implementing and analysing the power consumption of half adder and full adder circuits. There are different ways to implement a reversible adder. These different implementations depend on a balance between gates count, garbage outputs, ancillary bits and quantum cost.

A. ***Half adder using PERES gate***

A 1-bit half adder takes two binary inputs A, B and its outputs are described by the logic equations Sum = A XOR B, Carry = AB [7]. An existing reversible half adder can be constructed from two reversible gates and has one garbage bit: a Toffoli gate with the third input kept at zero and a Feynman gate. This gate combination corresponds to a single Peres Gate (PG) which acts as half adder as shown in Fig.10. The logical output of this half adder is verified by performing the simulation and its output is shown in Fig.11.

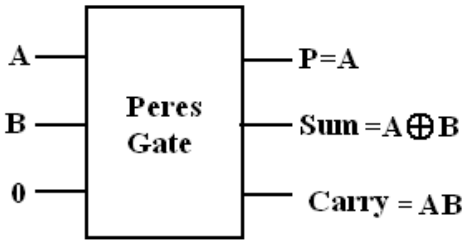

Fig.10. Reversible Half Adder using Peres Gate

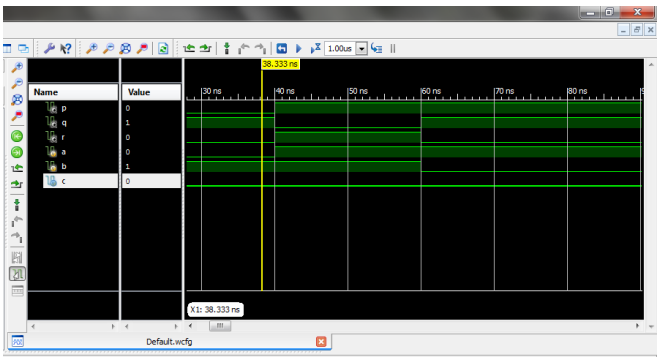

Fig.11.Simulation output of a Peres Gate Reversible Half adder

B. ***Half adder using IG Gate***

To implement a half adder using IG gate, there is need of two constant inputs forced to logic zero whereas it produces required sum and carry along with two garbage outputs G1 and G2. The schematic symbol of half adder using IG gate is shown in Fig.12, where Q is Sum, R is Carry, G1 and G2 are two garbage outputs[4].

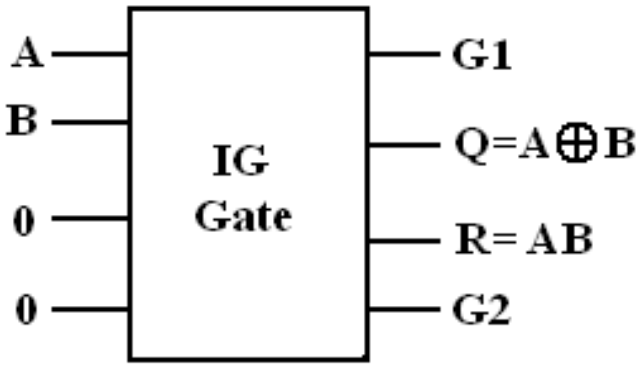

Fig.12. Reversible Half adder using IG Gate

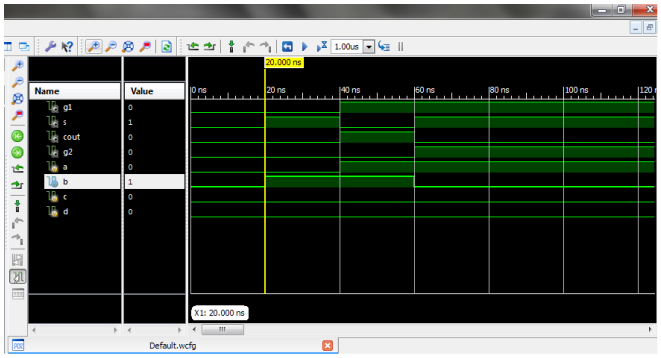

Fig.13.Simulation output of a IG gate Half adder

C. ***Full adder using PERES gate***

Full adder circuit can be designed using any of the above reversible gates discussed in literature [2], [3], [7]. The outputs Sum (S) and Carry (C_{out}) of a full adder circuit having three inputs A, B and C_{in} are described below.

$$S=A \oplus B \oplus C_{in}$$

$$C_{out} = (A \oplus B)C_{in} \oplus AB$$

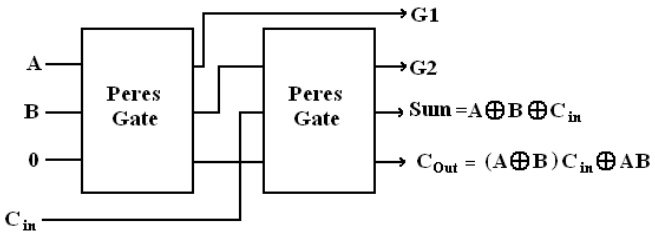

Fig.14.Reversible Full adder using Peres Gate

In this work, a few of the full adder circuits are implemented and power measurements are also made. Fig. 14. shows a full adder circuit with Peres gates[3] and its simulated output is shown in Fig.15.

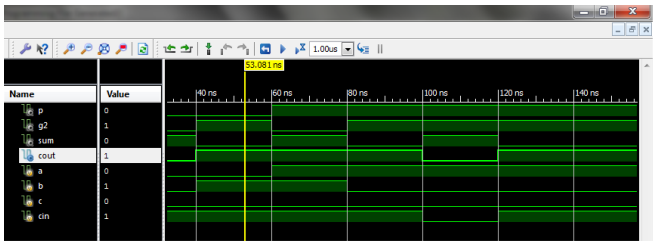

Fig.15.Simulation output of Peresgate Fulladder

D. ***Full adder using Online Testable Gate (OTG)***

A novel 4*4 reversible gate termed 'OTG' (Online Testable Gate) is suitable for providing online testability in reversible

logic circuits. OTG can work singly as a reversible full adder with bare minimum of two garbage outputs.

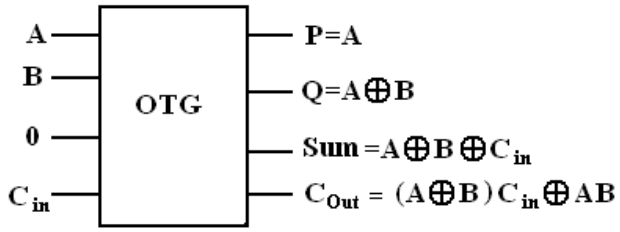

Fig.16.Reversible Full adder using OTG

This OTG gate is more efficient in reducing computational complexity[2]. Fig 16 shows the schematic diagram of a OTG as a reversible full adder with bare minimum of two garbage outputs(at least two garbage outputs will be required to realise a reversible full adder). The functionality of this OTG full adder is verified with the simulation output shown in Fig.17.

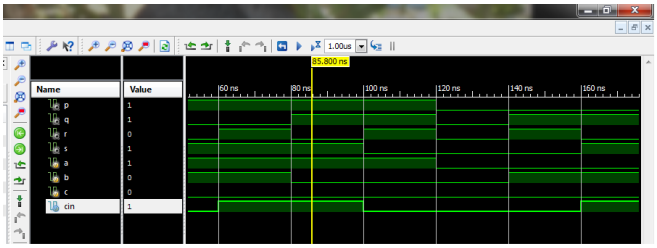

Fig.17.Simulation output of a OTG Full Adder

E. ***Full adder using IG gate***

Fig.18 shows the schematic diagram of full adder circuit using two IG Gates. It is implemented by keeping two constant inputs forced to logic zero resulting to produce a required Sum and Carry along with three garbage outputs G1, G2 and G3 [4]. The simulation output is shown in Fig.19.

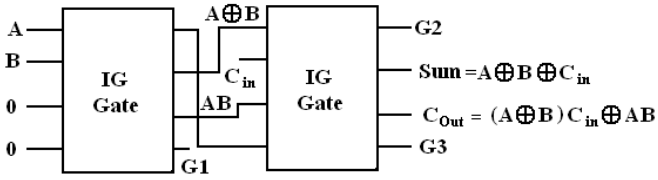

Fig.18. Reversible Full adder using IG Gate

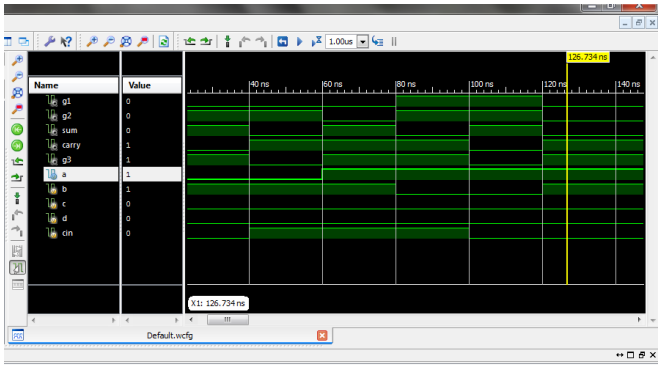

Fig.19.Simulation output of a Reversible Full adder using IG gate

IV. SIMULATION RESULTS OF POWER MEASUREMENTS

As mentioned above, the logical functionality of reversible logic gates like Feynman, Tofolli, Fredkin and Peres gates are verified. Further combinational circuits of Peres half adder, IG half adder, Peres full adder, OTG Full adder and IG full adder are implemented and their logical functionality is verified. The power measurements are made for half adder and full adder circuits implemented above using the Cadence Encounter(R) RTL Compiler shown in TABLE-I.

TABLE I Power measurements of half adder and Full adder Circuits

Name of the circuit	Power in nw
Reversible Half adder using Peres gate	248.94
Reversible Half adder using IG gate	439.15
Reversible Full adder using OTG gate	393.75
Reversible Full adder using Peres gate	659.14
Reversible Full adder using IG gate	906.95

V. CONCLUSION

In this work, first literature survey on reversible logic circuits in the area of basic reversible gates, difference from the existing boolean logic and conditions on reversible circuit design are focussed. Second, the various reversible logic gates like Feynman, Fredkin, Toffolli and Peres gates are implemented using the simulator tool Xilinx 12.3. Further a few reversible logic Half adder and Full adder circuits using reversible gates are also implemented. The functionality of the above circuits are verified using their simulated logical outputs. The power measurements are made using Cadence Encounter RTL compiler for all the above implemented circuits and their power consumption is analyzed in order to find the feasibility of further reduction in power consumption on the reversible logic elements resulting in enhancing the battery life of the portable application devices.

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