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Design and Analysis of Low Swing Conditional Capturing Flip-Flop for LC resonant Clock Distribution Networks

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ABSTRACT
The clock distribution network in digital integrated circuits distributes the clock signal which acts as a timing reference controlling data flow within the system. Since the clock signal has highest capacitance and operates at high frequencies, the clock distribution network consumes a large amount of total power in synchronous system. In this paper introduce a new flip-flop for use in a low swing LC resonant clocking scheme. The proposed low-swing differential conditional capturing flip-flop (LS-DCCFF) operates with a low-swing sinusoidal clock through the utilization of reduced swing inverters at the clock port. The functionality of the proposed flip-flop was verified at extreme corners through simulations with parasitic extracted from layout. The LS-DCCFF enables 6.5% reduction in power compared to the full swing flip-flop with 19% area overhead. The functionality of low-swing differential conditional flip-flop can be tested and verified using H-spice tool. Resonant clocking enables the generation of clock signals with reduced power consumption.

Keywords: Flip-flop, Delay, Low-swing, power, resonant clock, H-spice tool

INTRODUCTION:
In VLSI, the power dissipation of the clocking system, including clock distribution network and flip- flops, is often the largest portion of total chip power consumption.
Thus, it is important to reduce power Consumptions in clock trees. To reduce power consumption in clock distribution network, several small-swing clocking schemes have been proposed. Power consumption of a particular clocking scheme can be represented as

$$\mathbf{P}_{Ck\text{-}scheme}=P_{ck\text{-}network}+P_{FF} \quad (1)$$

Where $P_{ck\text{-}network}$ and P_{FF} represent power consumptions in the clock network flip- flops (FF), respectively each term in (1) can be represented as

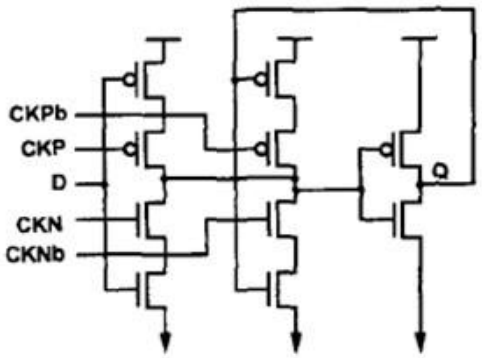
$$P_{ck\text{-}netwrk}=\{(C_{line}+C_{ck\text{-}tr}).V^2_{ck\ swing}\}.f_{ck} \quad (2)$$

$$P_{FF}=(\alpha_i.C_i.\gamma+\alpha_o.C_o.\gamma+C_{ckbuf}).V^2_{dd}\}.f_{ck} \quad (3)$$

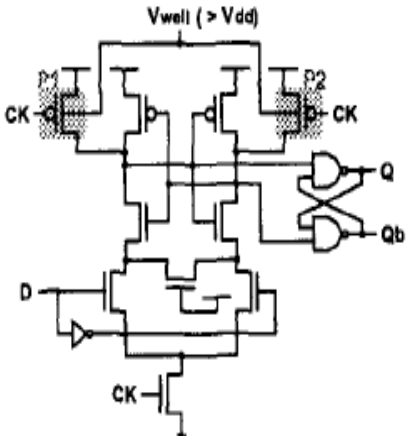
Where
C_{line} =Interconnect line capacitances,
$C_{ck\text{-}tree}$ = Capacitances of the clocked transistors of FF,
C_i = Internal node capacitances of the FF,
$C_{ck\text{-}buff}$ = Capacitances of the clock buffers of FF,
C_0 = Output node capacitances of the FF,
$V_{ck\text{-}swing}$ = Clock swing voltage level,
α_i= Internal node transition activity ratio, α_o = Output node transition activity ratio,
f_{ck}=clock frequency depends on triggering of FF.

Based on clocking the flip-flops can be classified three types 1) Conventional flip-flops 2) Energy recovery clocked flip-flops 3) Low swing LC resonant clocked flip-flops.
High performance of FF is obtained by increasing the frequency of clock. Power consumption increases by increasing the frequency of the clock. To reduce power consumption energy recovery is a technique originally developed for low power digital circuits. It achieves low energy dissipation by restricting current to flow across devices with low voltage drop by recycling the energy stored on their capacitors by using ac-type supply voltage.
Resonant clocking enables the generation of the clock signals with reduced power consumption. Lc resonant CDNs is to use the LC tank to drive the global clock distribution while the local square clock is being delivered through conventional buffers. So,this leads minor power savings in LC globally – resonant. In order to achieve maximum power savings,LC tank drive the entire global and local clock network.
Clock buffers are removed to allow the global and local clock energy to resonate between the inductor and entire clock capacitance. Thus enabling maximum power saving. This simplifies LC low- swing clocking. Since only reduced swing buffers are used at the Flip-Flop gate.
In this paper, A low-swing LC resonant differential conditional capturing flip-flop is proposed for use in low-swing LC resonant CDNs. The remainder of this paper is organized as follows
Section I describes the conventional flip-flops and their problems. Section II describes the energy recovery flip-flops, Section III describes the low swing LC resonant clocking and their simulation results

I.CONVENTIONAL FLIP-FLOPS:



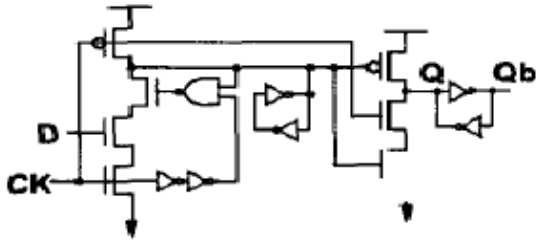
(a)



(b)

Fig.1: Conventional small-swing clocking flip-flops: (a) HSFF, (b) RCSFF.

The above Fig.1Shows the several Conventional small-swing clocking flip-flops. The half-swing flip- flop (HSFF) requires four clock signals, which suffers from skew problems among the four clock signals and incursadditional area as shown in Fig1(a).Two upper swing clocks (CKP, CKPb) are fed to PMOS transistors and the other two lower swing clocks (CKN, CKNb) are fed to NMOS transistors. Hence this scheme needs a special clock driver circuit which requires large capacitors. Also, this scheme increases the interconnect capacitance of clock networks and thus the power consumption. The speed degradation of the half swing scheme also cannot be ignored. Although a reduced clock-swing flip-flop (RCSFF) needs only one clock signal, it requires an additional high power supply voltage for well bias control *($V_{well} > V_{dd}$)* to reduce the leakage current as shown in Fig 1(b). Simple clocking scheme can be used forRCSFF



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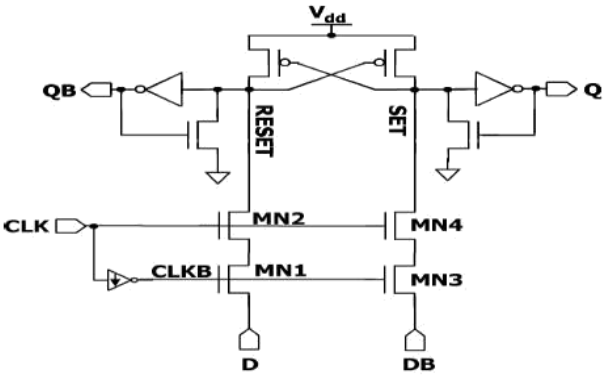

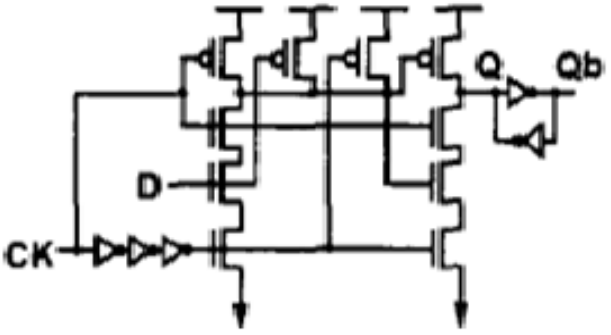

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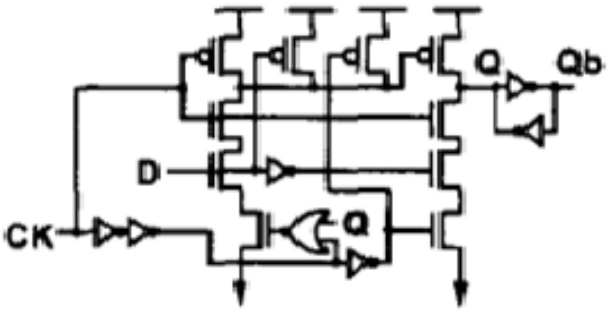


(c)

Fig. 2: Conventional high-performance flip-flops: (a) SDFF (b) HLFF and (c) CCFF.

The above Fig .2 shows the hybrid-latch flip-flop (HLFF) and semi-dynamic flip-flop (SDFF) have been known as the fastest flip-flops, but they consume large amounts of power due to redundant transitions at internal nodes. To reduce the redundant power consumption in internal nodes of high-

performance flip-flops, conditional capture flip-flop (CCFF) has been proposed. Furthermore, HLFF, SDFF, and CCFF use a full-swing clock signal, which causes significant power consumption in the clock tree.

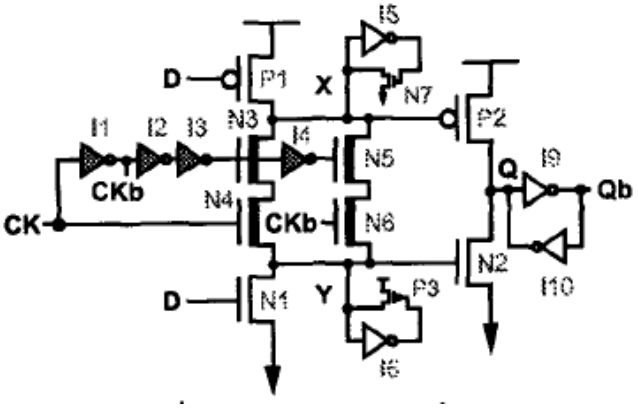
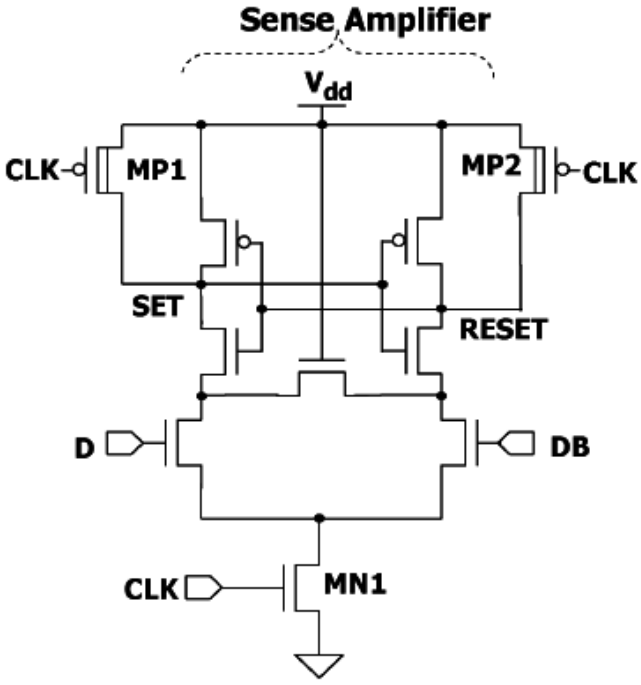


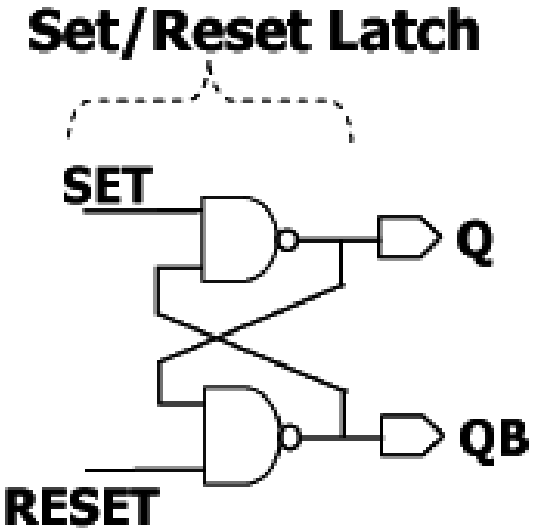
Fig 3. Schematic of LSDFF

Low Swing Double Edge Triggered Flip- Flop overcomes the problems of conventional flip- flops. A schematic diagram of low-swing clock double-edge triggered flip-flop(LSDFF) is shown in above Fig.3. Internal nodes X and *Y* are charged and discharged according to the input data D, not by the clock signal. Therefore, internal nodes of LSDFF switch only when the input changes and inherently do not need a conditional capture mechanism similar to that in pulse-triggered TSPC flip-flop (PTTFF). In PTTFF, either one of the data- precharged internal nodes is in floating state, which may cause malfunction of the flip-flop. Also, its internal node does not have a full voltage swing, which causes performance degradation. To remove these shortcomings, two latches were introduced in LSDFF. The use of one inverter and one transistor pairs (half-keeper) reduces fighting current, thus reducing the latency and power consumption.

II: ENERGY RECOVERY CLOCKED FLIP- FLOPS:



(a)



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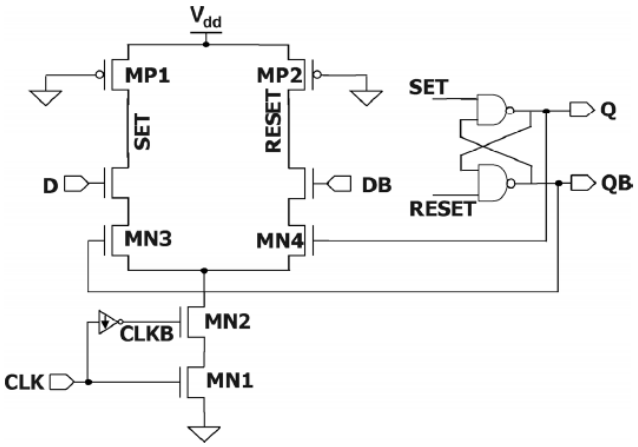
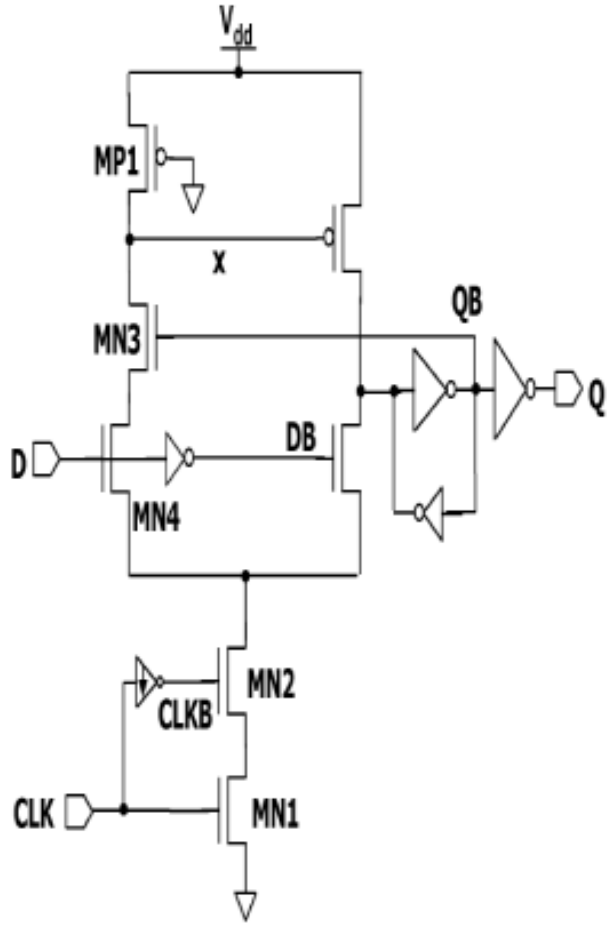


(c)



(d)

Fig 4: Energy recovery clocked Flip-Flops (a) SAER (b) SDER (c) DCCER (d) SCCER.

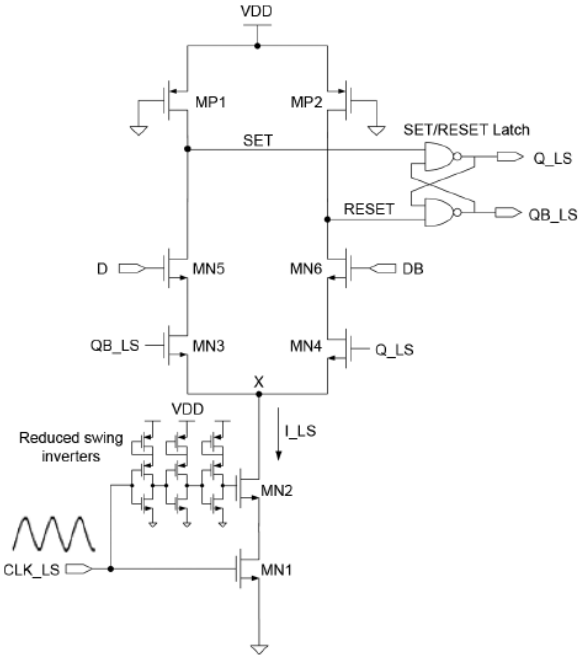
TheFig.4 shows the energy recovery clocked flip-flops. The Fig4.(a) represents SAERFF. It is a dynamic flip-flop with precharge and evaluate phases of operation. This flip-flop is used to operate with a low-voltage-swing clock. SAER flip-flop to operate with an energy recovery clock. When the clock voltage exceeds the threshold voltage of the clock transistor (MN1), evaluation occurs. At the onset of evaluation, the difference between the differential data inputs (D and DB) results in an initial small voltage difference between SET and RESET nodes. This initial small voltage difference is then amplified by the cross coupled inverter and as a result either SET or RESET switches to low. This state transition is captured by the set/reset latch (cross coupled NAND gates) and retained for the rest of the cycle time until next evaluation occurs.

The above Fig.4(b). Shows the SDER is static pulsed flip-flop. The clock signal and the inverter output (CLKB) are applied to transistorsMN1andMN2 (MN3 and MN4). The series combination of these transistors conducts for a short period of time during the rising transition of the clock when both the CLK and CLKB signals have voltages above the threshold voltages of the nMOS transistors. Since the clock inverter is skewed for fast high-to-low transitions, the conducting period occurs only during the rising transition of the clock, but not on the falling transition. In this way, an implicit conducting pulse is generated during each rising transition of the clock. This flip-flop is static because SET and RESET nodes statically retain the state of the flip-flop without being precharged. The static nature of the flip-flop ensures that there is no internal redundant switching on SET and RESET nodes if input data remains idle.

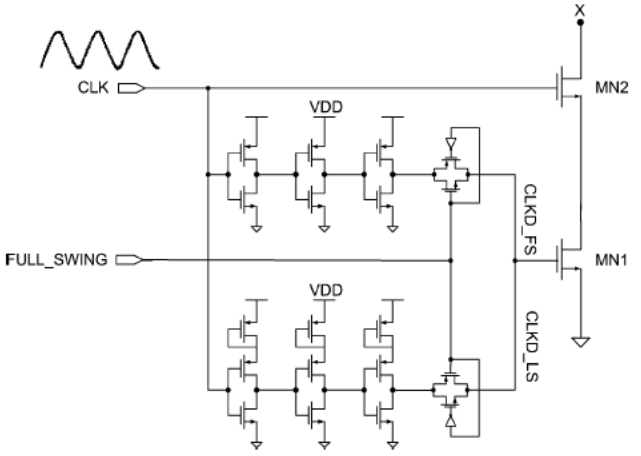
The above Fig.4(c) shows the differential conditional-capturing energy recovery (DCCER) flip-flop. Similar to a dynamic flip-flop, the DCCER flip-flop operates in a precharge and evaluate fashion. However, instead of using the clock for precharging, small pull-up pMOS transistors (MP1 and MP2) are used for charging the precharge nodes (SET and RESET). The DCCER flip-flop uses a NAND-based set/reset latch for the storage mechanism. The conditional capturing is implemented by using feedback from the output (Q and QB) to the control transistors MN3 and MN4 in the evaluation paths. Therefore, if the state of the input data (D and DB) is same as that of the output (Q and QB), both left and right evaluation paths are turned off preventing SET and RESET from being discharged. This results in power saving at low data switching activities when input data remains idle for more than one clock cycle.

The above Fig.4(d) shows a single-ended conditional capturing energy recovery (SCCER) flip-flop. SCCER is a single-ended version of the DCCER flip-flop. The transistor MN3, controlled by the output QB, provides conditional capturing. The right-hand side evaluation path is static and does not require conditional capturing.

III. LOW SWING LC RESONANT CLOCKING:



(a)



(b)

Fig. 5 (a) LS-DCCFF (b) Modification to enable full- and low-swing flip-flop clocking.

The above Fig. 5(a) shows the proposed LS-DCCFF. Conditional capturing is used to minimize power at low data switching activities by eliminating redundant internal transitions, reduced swing inverters are fed by low swing sinusoidal clock signal. This is done to reduce short circuit power. The load pMOS transistor in the reduced swing inverters is always in saturation since Vgs=Vds It lowers the voltage at the source of the second pMOS in each inverter to approximately VDD− *Vtp* thus turning it off when the low-swing sinusoidal clock signal reaches its peak voltage. The peak voltage for the low-swing clock was chosen less than VDD.

The above Fig.5(b) shows the LS-DCCFF was modified at node _ to allow the operation under full-swing and low-swing clocking. When signal *FULL_SWING* is high, full-swing clocking is enabled and the inverted clock output of the normal inverters *CLKD_FS* is feeding transistor *MN1*. Whereas low-swing clocking is enabled when signal *FULL_SWING* is low and the output of the reduced voltage swing inverters *CLKD_LS* feeds transistor *MN1*.

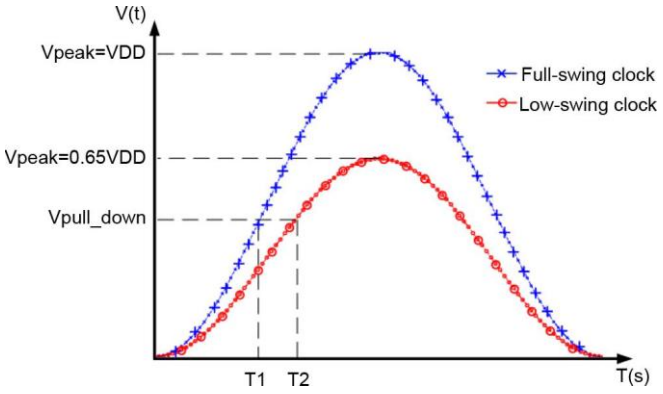


Fig 6 : Delay between the low- and full-swing clock signals to reach V pull down

TABLE I Max. power, delay and PDP of different flip-flops

Name of the FF	MAX.POWER (mw)	DELAY (ps)	PDP
SAER	3.225	293.45	$0.9463X10^{-12}$
SDER	10.38	183.46	$1.9043X10^{-12}$
DCCER	3.214	185.36	$0.59574X10^{-12}$
SCCER	11.73	130.92	$1.53569X10^{-12}$
SDFF	13.06	3.448	$0.0450X10^{-12}$
HLFF	5.582	1907	$10.6448X10^{-12}$
CCFF	6.046	1506	$9.1052X10^{-12}$
HSFF	6.702	18.486	$0.5930X10^{-12}$
RCSFF	7.014	1909	$1.3389X10^{-12}$
LSDFF	21.82	88.657	$1.93449X10^{-12}$
LSDCFF	0.744	269.52	$0.20652X10^{-12}$
LSDCFF-P	0.8812	302.69	$0.2667X10^{-12}$

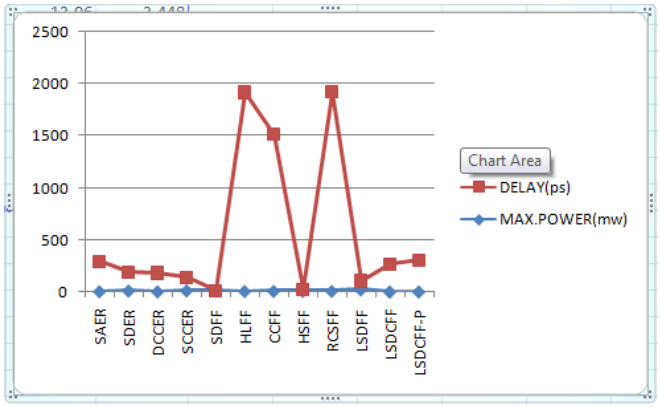


Fig.7 Power and delay comparisons of different flip-flops.

CONCLUSION:

Maximum power is reduced in low-swing differential conditional capturing flip-flops compared to all other conventional flip-flops. Low-swingresonant clocking in pulsed flip-flops results in a delayed flip-flop response. The functionality of the proposed flip-flop has been investigated through HSPICE simulation in a 90-nm.

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