International Journal of Applied Engineering Research ISSN 0973-4562 Volume 10, Number 14 (2015) pp 34042-34046

FPGA Implementation of Multi-Bit Flip-Flop Based on Power Optimization Technique

[1]Kareti Pamulu, [2]B Murali Krishna, [3]G L Madhumati, [4]Habibulla Khan

[1]M.Tech Student of VLSI, Department of ECE, K L University,Vaddeswaram
kareti.359@gmail.com
[2]Assistant Professor, ECE Department, K L University,Vaddeswaram-522502 muralikrishna@kluniversity.in
[3]Professor and Head of ECE Department, DIET, Vijayawada
[4]Professor and Dean, Department of ECE, K L University

Abstract
In modern VLSI designs, power consumed by clocking has taken a major part of the entire design. In VLSI circuits clock is the most dominating power consuming element. To achieve the optimum power, it is need to reduce the clocking power. This paper describes a method for reducing the power consumption by replacing some flip flops with fewer multi-bit flip flops. Concept of merging flip flops is implemented in a simple storage device. Proposed work will reduce the power when compared to the conventional system.

Keywords: Latches, Flip-Flops, Verilog-HDL

1. INTRODUCTION

Nowadays, achieving low power consumption is a tedious one in IC fabrication industries which needs a faster clock which increases power dissipation. The Clock-Tree-Synthesis is the process of insertion of buffers or inverters along the clock path of ASIC design in order to achieve zero/minimum skew or balanced skew Large clock skew can force the designer to use large time period between clock pulses which make the system to perform slower. Usually clock trees are created by using buffers or inverters. Building a inverter clock tree would use less FFT's than building buffer clock tree to urge a similar target clock skew. Thus it might get less power consumption and delay. Hence to reduce the power consumption several low-power design techniques are adopted such as gated clock and making multi-supply-voltage styles, minimizing clock network and dynamic voltage/frequency scaling. With these techniques minimizing clock network is extremely vital in reducing power consumption as a result of it accounts for up to 45% of dynamic power of the chip. So in this clock system 90% of the power is consumed by the flip-flops themselves and also the last branches of the clock distribution network that directly drives the flip-flops. Thus the single bit flip-flop are used and every flip-flop needs a separate clock buffers which consumes large power. The remaining paper is structured as; the Section 2 describes the conventional flip-flop and their drawbacks. The section 3 will explains about the proposed method and section 4 describes the implementation details. Section 5 and Section 6 describes the simulation analysis and conclusion respectively.

2. CONVENTIONAL SYSTEM

A flip-flop is a single bit memory storage element, which is very similar to a latch in that it is a bi-stable device which having two states and a feedback path that allows it to store a one bit of information. The variation between latch and flip-flop is that a latch is level triggered and the flip-flop is edge triggered. Flip-flops are classified into several different types each with its own uses and operations. Flip-flops are of four different types such as SR, D, JK, and T. In conventional type each flip-flop requires a separate clock source which increase the clocking power considerably also the area and clock skew will get increased which is shown in fig.1

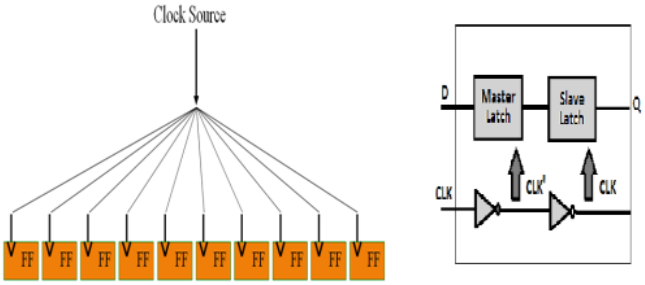

Fig.1 (a) Path From Clock Source to Clock Sink (b) Single-Bit Flipflop

Fig.1(b) shows a single bit flip-flop it has two latches (Master Latch and Slave Latch). The latches need CLK signal to trigger the device. In order to have better delay from CLK to Q, CLK is regenerated from CLK. So two inverters are placed in the clock path.

3. PROPOSED SYSTEM

The aim of the present work is therefore to propose the Multi-bit flip-flops which merge the single bit flip-flop that share the clock buffers. As CMOS technology improves, the driving capability of an inverter-based clock buffer rises. Thus driving capability of a clock buffer can be evaluated by the number of minimum-sized inverters that it can drive on a given rising or falling time. Due to manufacturing ground rules inverters in flip-flops tend to be increased in size. So as we get into micro

technology like 65nm and beyond the least size of clock driver can drive more than single flip-flop.

The advantages of Multi-bit flip-flops are:
1. Design area is being small
2. Needs less power and delay
3. Controllable clock skew
4. Improve in routing resource utilization

According to section 2, among those flip-flops; D flip-flop is chosen for this project because of low power consumption and its simplicity. The merging of 2 single bit flip-flops have been shown in Fig 2.

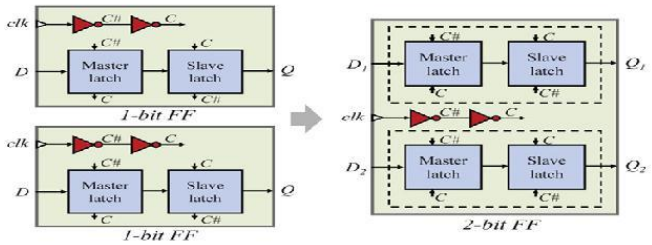

Fig.2 Merging of Flipflops (a) 2-Single Bit Flip-flop (before merging) (b) 2-Bit Flip-flop (after merging)

In this section, we introduced the multi-bit flip-flop concept. Before that we will discuss about single-bit flip-flop Fig: 2 shows an example of merging two 1-bit flip-flops into one 2-bit multi bit flip-flop. Fig 2(a) describes replacement of two 1-bit flip-flops by the 2-bit flip-flop as shown in Fig. 2(b) total power consumption can be reduced because the two 1-bit flip-flops can share the same clock buffer. Merging single-bit flip-flops into one multi-bit flip-flop can avoid additional inverters and reduces the total clock dynamic power consumption. Also the total area occupied by the flip-flops can also be reduced. The Fig 3 shows the flow chart of proposed work. Our proposed work is roughly divided into three steps. First step is identifying merge-able flip-flops, Build a combination table, and Merge flip-flops. In first stage, we have to identify the flip-flops which are supposed to be combined. And in second stage, a combination table can be formed, which defines all possible combinations of flip-flops in order to get a new multi-bit provided by library. In third stage, the flip-flops can be merged with the help of the table.

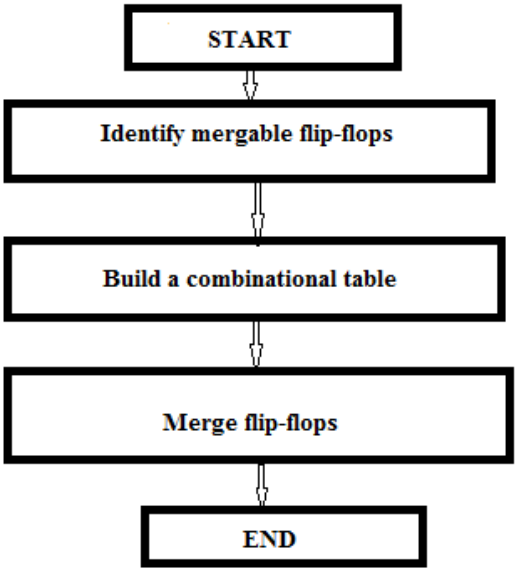

Fig.3 Proposed System Flow Chart.

3.1 Identifying Merge able Flip-Flops

Multi-bit flip-flop cells are capable of decreasing the power consumption due to sharing of common inverters internally done in the flip-flop. At the same time they can reduce the clock skew.To obtain these benefits, the ASIC design must meet the following requirements. Thus the single-bit flip-flops want to be replace with multi-bit flip-flops must have same clock condition and same set/reset condition.We may have so many combinations to form a single multi-bit flip-flop. For example, consider that we have to build a 4-bit flip-flop we may have 3 combinations to setup that, i.e. by merging four 1-bit flip-flops else by merging two 2-bit flip-flops or else it can be formed by merging one 3-bit and one 1-bit flip-flop.

4. IMPLEMENTATION DETAILS

We implemented this concept in a simple 4bit register circuit and also analyzed the power consumption. This as shown in figure.4 and proposed Multibit flip-flop design is shown in figure 5. In this four single bit flip-flops are used, which requires four separate clock drivers. In our proposed work the multi-bit flip-flop concept is implemented in the register, which requires single clock driver to drive them and the corresponding power consumption is measured.

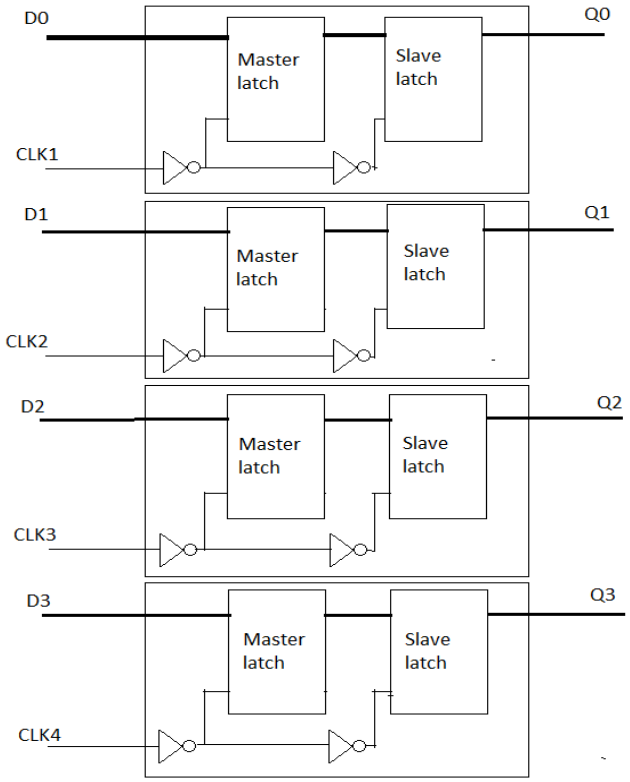

Fig. 4 A Simple 4-bit Register Circuit

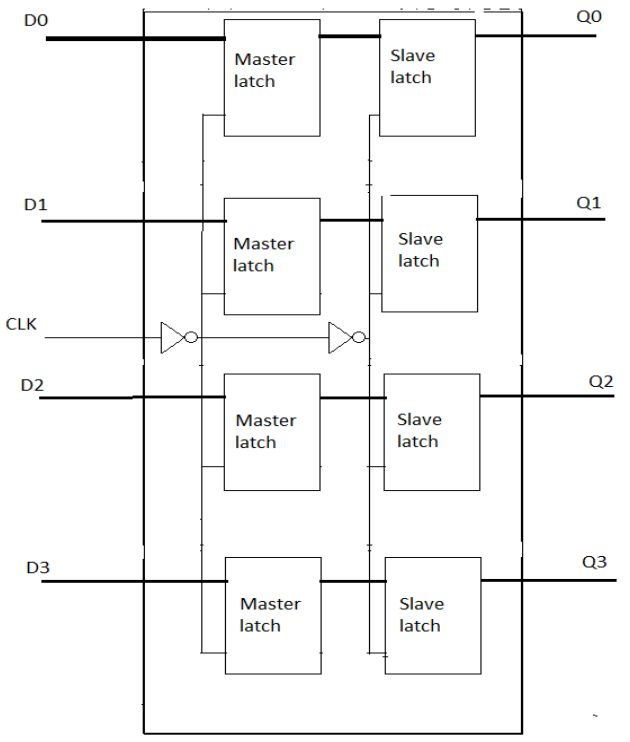

Fig.5 Proposed 4-bit Multibit Flip-Flop

5. RESULTS & DISCUSSION

We implemented the concept in Verilog HDL and are executed by Xilinx ISE Design suit with Modelsim simulator. Results for the power differences between existing system and proposed system is shown in the below figures.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		72
Vccint 1.20V:	22	27
Vccaux 2.50V:	12	30
Vcco25 2.50V:	6	16
Clocks:	5	6
Inputs:	2	2
Logic:	0	0
Outputs:		
Vcco25	5	12
Signals:	0	0
Quiescent Vccint 1.20V:	16	19
Quiescent Vccaux 2.50V:	12	30
Quiescent Vcco25 2.50V:	2	4

Fig.6 Power Consumption of Existing System

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		69
Vccint 1.20V:	19	23
Vccaux 2.50V:	12	30
Vcco25 2.50V:	6	16
Clocks:	3	3
Inputs:	1	1
Logic:	0	0
Outputs:		
Vcco25	5	12
Signals:	0	0
Quiescent Vccint 1.20V:	16	19
Quiescent Vccaux 2.50V:	12	30
Quiescent Vcco25 2.50V:	2	4

Fig.7 Power Consumption of Proposed System

Existing System	Proposed System
72(mW)	69(mW)

Fig.8 Power Comparison

Synthesis Report	Existing System		Proposed System	
No.of Slices	4	0%	4	0%
No.of Slice Flipflops	8	0%	8	0%
No.of four I/P LUTs	4	0%	2	0%
No.of IOs	13	-	11	-
No.of Bounded IOBs	13	12%	11	10%
No.of GCLKs	4	16%	2	8%

Fig.9 Synthesis Report

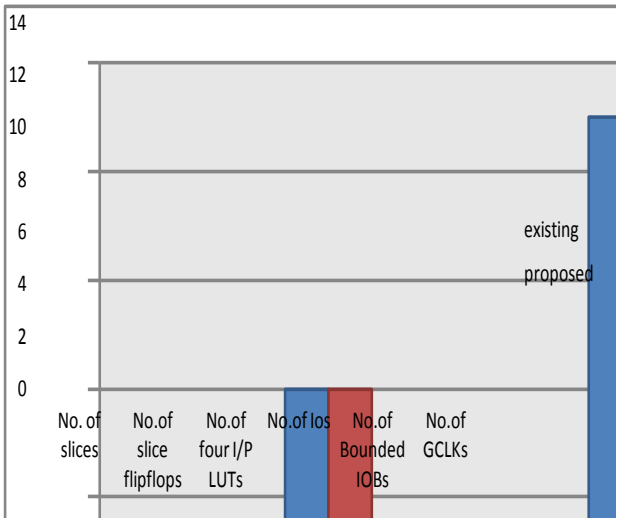

Fig.10 Graphical Representation

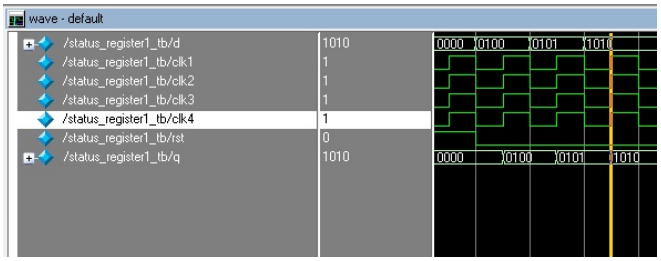

Fig.11 Simulation Results obtained for 4-bit Register Using Single Bit Flip-Flop

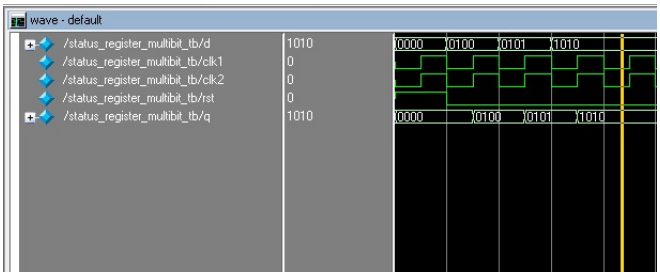

Fig.12 Simulation Results Obtained for 4-bit Multi Bit Flip-Flop

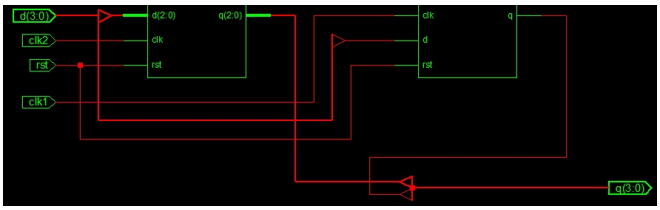

Fig.13 RTL Schematic of Proposed System

CONCLUSION

In this paper, the concept of multi-bit flip-flops is introduced for the replacement of single-bit flip-flop which achieves the reduced power consumption in a circuit. Simulation and synthesis results have been observed by using ModelSim and XILINX XST tool. The proposed work have achieved the less power consumption when compared to the conventional system.

REFERENCES

[1] *"Effective and Efficient Approach for Power Reduction by Using Multi-Bit Flip-Flops,"* Ya-Ting Shyu, Jai-Ming Lin, Chun-Po Huang, Cheng-Wu Lin, Ying-Zu Lin, and Soon-Jyh Chang, *Member IEEE*. IEEE transactions on very large scale integration (vlsi) systems, vol. 21, no. 4, april 2013.

[2] D. Duarte, V. Narayanan, and M. J. Irwin, *"Impact of technology scaling in the clock power,"* in *Proc. IEEE VLSI Comput. Soc. Annu. Symp.*, Pittsburgh, PA, Apr. 2002, pp.s 52–57.

[3] H. Kawagachi and T. Sakurai, *"A reduced clock-swing flip-flop (RCSFF) for 63% clock power reduction,"* in *VLSI Circuits Dig. Tech. Papers Symp.*, Jun. 1997, pp. 97– 98. Y. Cheon, P.-H. Ho, A. B. Kahng, S. Reda, and Q. Wang, *"Power-aware placement,"* in *Proc. Design Autom. Conf.*, Jun. 2005, pp. 795–800.

[4] Y. Cheon, P.-H. Ho, A. B. Kahng, S. Reda, and Q. Wang, *"Power-aware placement,"* in *Proc. Design Autom. Conf.*, Jun. 2005, pp. 795–800.

[5] P. Gronowski, W. J. Bowhill, R. P. Preston, M. K. Gowan, and R. L. Allmon, *"High-performance microprocessor design," IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 676–686, May 1998.

[6] W. Hou, D. Liu, and P.-H. Ho, *"Automatic register banking for lowpower clock trees,"* in *Proc. Quality Electron. Design*, San Jose, CA, Mar. 2009, pp. 647–652.

[7] Y.-T. Chang, C.-C. Hsu, P.-H. Lin, Y.-W. Tsai, and S.-F. Chen, *"Post-placement power optimization with multi-bit flip-flops,"* in *Proc. IEEE/ACM Comput.-Aided Design Int. Conf.*, San Jose, CA, Nov. 2010, pp. 218–223.