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Pulsed CMOS Neural Network Design in Subthreshold Region using Translinear Principle

Ayyavoo Mithila and Vijayakumari Valsalam

Ayyavoo Mithila, Department of Electronics and Communication Engineering,
Sri Krishna College of Technology, Coimbatore-641042, India
(e-mail: mithila6@ gmail.com)
Vijayakumari Valsalam is with Department of Electronics and Communication Engineering,
Sri Krishna College of Technology, Coimbatore-641042, India
(e-mail: v.vijayakumari@skct.edu.in)

ABSTRACT
Analog neural network (ANN) design based on CMOS circuits working in subthreshold region related to translinear principle and pulse stream technique is reviewed. We briefly explain the basic concepts of the following: Neural Networks based on pulse stream technique, Subthreshold region of operation with their circuits and Translinear circuits. These techniques are used in unification. First, research relating to the multiplier design and their simulation results are reviewed. Then, relevant activation function circuit designs are discussed. Finally, research relating analysis of circuit level design of the neural network and modeling are discussed. In simpler form, the research shows that pulse based ANN in subthreshold region constituting of multipliers and activation functions based on current mode maybe used for achieving reasonable bandwidth and power.

Keywords: Analog Neural Network, CMOS Design, Current mode, Pulse stream technique, Subthreshold region of operation, Translinear Principle.

1. INTRODUCTION

A general view of biological neuron anatomy is categorized into dendritic tree, neuron and axon. The synaptic stimulation may generate action potential as a result of electrical responsein neurons [1, 2].Pulse bursts are produced by some neurons with longer or defined intervals [3]. Synaptic activity, cell morphology and electrical properties of membrane in the dendrite of neuronestablish the behavior of the pulse [3].
Analog VLSI neural computation has been a popular field of research. The VLSI implementation of artificial neural network models can be made with relevant designs of synapse multiplier and neurons with activation functions. Asynchronous approachhas beenconsidered with reference to modeling of neuron compatibility to synapse design [4, 5, 6, 7, 8, 9].
With combination of analog and digital functionalities, ICs integrate an entire system as a whole on a single chip [10].CMOS technology has the advantages of using minimal power with good computational density and computer-aided design [CAD] technologies help in automation of circuitry [11, 12]. In case of analog designing, it is important to realize the boundaries of circuit geometries while simulating on computer rather than designing on bread board[13].
Our survey is done for optimal design of current mode pulsed neural networks with CMOS devices using translinear principle that works in subthreshold or weak inversion region. It would lead to interesting vision applications with low power and reasonable bandwidth.
Here, Section 2 discusses the background which surveys concepts of neural networks using pulse stream technique, subthreshold region of operation and its circuits and translinear principle for MOSFETs. Sections 3 and 4 discuss literature on analysis of options of current mode CMOS multipliers and activation functions with their derivatives that use translinear principle and working in subthreshold region. Section 5 discusses few literatures on analog neural networks based on translinear principle working in subthreshold region.

2. BACKGROUND

2.1 Neural networks based on pulse stream technique

A current-mode based pulse width modulation(PWM) analog neural network made of fixed components has been designed and analyzed that can be used for implementation of VLSI neural systems [14]. Pulse streams pass on analog information on time axis [3, 15, 16].
Essential functional designs for handling weights, synaptic multiplication, addition, activation functions and communication of input and output activities amongst neurons are required for conventional multi-layer perceptron (MLP) design [3, 17, 18].For analog neurons, the modulation technique is used for communication[4, 19, 20].
A weight storage technique like that of compact weight-increment circuit allows advantage of speed in on-chip learning [17, 18, 21 22, 23, 24, 25, 26, 27].This has been achieved by design of simple bias circuits that eliminates the temperature dependence to make the circuits suitable for real-world applications [4, 28, 29].

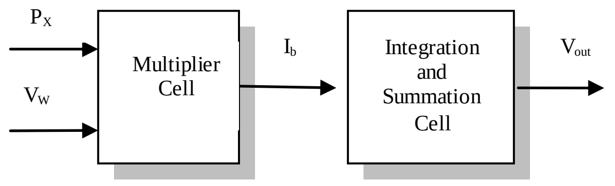

Figure 1. Generalized PWM Synapse Multiplier-Voltage mode

In PWM based technique, pulses generated represent multiplication as the "postsynaptic pulses of a width in time is proportional to the synaptic weight and at a frequency controlled by the presynaptic neural state" [30, 31].
A generalized structure for design of synaptic multiplier maybe noticed in Fig.1 with input pulse P_x, weight voltage V_w, I_b the intermediary current and converted to output voltage V_{out}[32, 33].For achieving compactness, simplicity and robustness of signals, pulse stream technique is used in the design of efficient analog computations with disadvantage of high value of currents on power supply lines [30, 31].
The weighted summation operation is done by switching current, controlled by a pulse width control value that is relative to current input [14, 34]. In a current mode neural network, pulses of current are added that results in twice the size of the every pulse with no loss of information if the pulses are integrated to preserve the integrity of current[4, 34]. Current maybe accumulated as capacitor charge or on integrator, based on operational amplifier circuit [30].
Analog pulsed multiplication and activation functions are usually based on non-linear amplifiers of pulse stream data transmission in analog [3]. Synaptic multiplication and activation functions have to be designed and used to work along pulse stream analog techniques where neural states are represented as sequence of pulses [35]. Networks maybe implemented using asynchronous analog pulse stream devices [16, 36].
It is important to take notice of a test-chip that considers three issues for design of analog neural network viz., pulse stream multiplication, least value for handling weight and activation function as "sigmoid-prime''[30, 37]. This circuit shows possibility of implementing in VLSI within acceptable limits of performance [30, 37, 38, 39].

2.2 Subthreshold region of operation and its circuits

Biomedical applications for which current levels are required to be extremely small include pacemakers and implantable devices that operate for longer duration with small nonrechargeable batteries[40]. As we are interested in pulsed neural networks, the circuits as explained in the subculture of pulsed neural CMOS design methods, the circuits working in subthreshold MOSFET operation are significant [4, 12, 22, 31, 41, 42, 43, 44]. While analyzing MOSFET equations, the drain-source current I_D is zero for $V_{GS} \leq V_t$. But they continue to pass current from drain to source. In this region of operation, drain-source current I_D depends exponentially on gate-source voltage V_{GS}:

$$I_D \; \alpha \; e^{KV_{GS}} \; (1)$$

where K depends on transistor operation in weak inversion region. The following equations for current in MOSFET's with the voltages V_{GS}, V_{SB}, V_{DB} with respect to the substrate and I_0 depends on mobility and other silicon physical properties [45, 46, 47, 48].
For an NMOS transistor in weak inversion,

$$I_D \equiv I_{DS}$$

$$I_D = I_0 \frac{W}{L} e^{\left(K_n \frac{V_{GB}}{V_t}\right)} \left(e^{-\frac{V_{SB}}{V_t}} - e^{-\frac{V_{DB}}{V_t}}\right) \; (2)$$

and for a PMOS transistor,

$$I_D \equiv I_{SD}$$

$$I_D = I_0 \frac{W}{L} e^{\left(-K_p \frac{V_{GB}}{V_t}\right)} \left(e^{\frac{V_{SB}}{V_t}} - e^{\frac{V_{DB}}{V_t}}\right) (3)$$

The relationship in Eq.1 allows circuits developed for bipolar transistors whose input-output relationship can be directly adapted in MOSFETs and the small currents involved reduce the power consumption in subthreshold devices [45]. The trade-off is in terms of noise immunity but tolerable noise can be helpful in neural computation as same as biological nervous system [4, 40, 49].
The mismatch characteristic of MOS transistors with decreasing drain currents also complicates the design [50, 51, 52, 53, 54, 55, 56]. Even weak inversion models used in simulation programs such as SPICE have major limitations [40].

2.3 Translinear Principle

A group of analog circuits was described as the 'translinear' group whose main function is their precise proportionality of transconductance to collector current in BJTs that result in temperature-insensitive behavior [57]. The basic translinear principle states that:
"In a closed loop containing an equal number of oppositely connected translinear elements, the product of the current densities in the elements connected in the Clockwise (CW) direction is equal to the corresponding product for elements connected in the Counter Clockwise (CCW) direction".

Translinear circuits operate entirely in the current domain; voltage variations due to the signals are small [57, 58, 59, 60, 61, 62, 63, 64]. They can generate algebraic functions that can incorporate products, quotients, power terms with fixed exponents, that may be integral or nonintegral, positive or negative, and sums and differences [59, 64, 65, 66, 67, 68, 69, 70, 71, 72].
Circuits like current-conveyors[73], associative memory and silicon retina are used as examples with relevant analogies to physics and organization of information processing in the nervous system[74, 75, 76, 77, 78, 79].
Some significant contributions can be observed for our design methodology with implementation of "neuromorphic" analog network designs [80, 81, 82, 83, 84, 85, 86, 87, 88].

Fit to our design methodology the following contributions are most relevant

(i) Analog input-output interface, weight coefficients, and adaptation blocks are all integrated on the chip fabricated in n-well double-polysilicon, double-metal CMOS process [81].

(ii) A comprehensive overview aiming at neuromorphic analog network computations on VLSI results in design of analog subcircuits with components of limited precision when put together as networks, can successfully perform linear and non-linear computation effectively [62, 83].

The relevance of subthreshold region to transistors exhibits I_D exponential variation with respect to gate voltage with translinear principle to describe the functionality [62, 89, 90].

3. ANALYSIS OF MULTIPLIERS

The Synapse Multiplier design that is relevant to our objective should work in current mode [91, 92, 93, 94, 95, 96, 97, 98] subthreshold region [99, 100] and translinear principle[101, 102, 103].

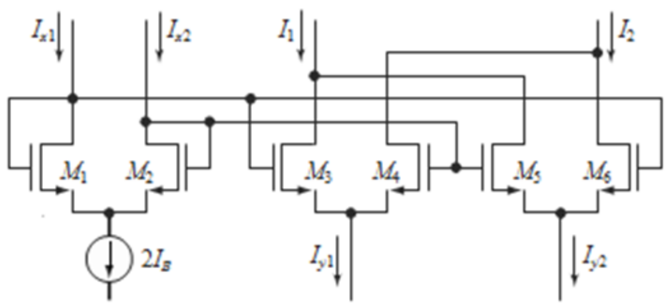

Figure 2. Generalized current mode weak inversion CMOS Multiplier [29]

There have been profoundcontributions for such design with relevant criteria and such an analysis becomes necessity keeping pulse stream technique in mind [4, 17, 37, 104].

In Fig.2, the general TLP is followed for the design of multiplier in weak inversion region wherein I_b the bias current, $I_x$and $I_y$are the signal currents, and $I_D$is the drain-to-source current of MOSFET with I_{x1}, I_{x2}, I_{y1} and I_{y2} as input currents [29, 102, 105, 106].

$$V_{gs1} + V_{gs4} = V_{gs2} + V_{gs3} \quad (4)$$

$$V_{gs1} + V_{gs6} = V_{gs2} + V_{gs5} \quad (5)$$

whereVgs is the gate-to-source voltage.

$$I_{out} = \frac{2I_x I_y}{I_B} \quad (6)$$

TABLE I PARAMETERS IN VARIOUS ANALYSES OF CURRENT MODE TRANSLINEAR FOUR QUADRANT MULTIPLIER CIRCUITS IN SUBTHRESHOLD REGION

Paper	Supply voltage V	Power Dissipation µW	Bandwidth Hz	Other parameters	Technology used
[126]	0.5	84	30K	I_b=370nA	--
[127]	2	5.5	200K	I_b=250nA THD<0.9%	0.35µm
[29]	1	1.2	768K	I_b=100nA THD = 1.3%	0.18µm Level 53 BSIM3v 3.2
[123]	3	60	58M	I_b=10 µA THD = 3.06%	0.5µm CMOS 40V Process
[119]	±0.75	2.3	2.8M	THD = 0.7%	0.35µm TSMC CMOS Process
[120], [121], [122]	±0.75	2.3	2.3M	THD = 1.1%	0.35µm TSMC CMOS Process
[96]	1.8	<207	31.2M	THD=1.24%	0.18µm HSPICE Level 49

V = Volts, W= Watt, Hz = Hertz; A = Ampere

For basic understanding of multipliers, it is relevant to understand two versions of the circuit configuration for MOS four-quadrant multiplier circuit that has been based on square-law characteristics with different bandwidth of 1 MHz and 4.5 MHz respectively [107]. The dynamic behavior of these multipliers were simulated and analyzed to signify use of accurate design models and some process variations [108, 109, 110]. Low voltage multiplier using the principle has been designed with low voltages [111, 112, 113].

Current mode analog multiplier based on translinear principle[114] with operating region of the cell being limited by the validity of the exponential dependency and leakage currents that gives basic idea of multiplier cell and their errors [115].

With little modifications in circuit, it can be made to work as a squarer or a divider [116, 117, 118, 119, 120, 121, 122]. The body effect of NMOS transistors that is capable of introducing nonlinearity error and its elimination by modifying the multiplier topology with PMOS transistors [123]. An analog design of multiplier has been simulated and verified for high linearity by adopting the adaptive bias technique to the differential pair [29, 124, 125].

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Mismatch model for multipliers should also be considered while designing current mode multipliers that uses subthreshold MOSFETs with translinear loops accounts for non-linearity and accuracy in transistors [50, 51, 52, 53, 55].

For our purpose of multiplier design that adopts Gilbert's translinear principle to weak inversion in current mode, we refer to some options available in literature in Table I. We notice that the power dissipation (PD) of 1.2µW with bandwidth (BW) of 768KHz designed with 0.18µm technology might be quite favourable for our design [29]. Ideas maybe borrowed from designs with PD of 2.3µW and BW greater than 2MHz may help in achieving our objective of reasonable PD and BW, but with 0.18µm technology instead of 0.35µm technology [119, 120, 121, 122]. Other relevant papers show optimal THD (total harmonic distortion) values.

4. ANALYSIS OF ACTIVATION FUNCTION AND THEIR DERIVATIVES

For the purpose of introducing non-linearity into the network, activation function for hidden units plays a pivotal role. With nonlinearity, hidden layers would make powerful networks than just plain perceptrons[128, 129]. Generally, activation functions like piecewise linear, sigmoid, hyperbolic tangent functions and their derivatives exist in use. Gaussian functions are also in use [130, 131].The bounding property, computability speed, and mathematical properties of activation functions in the realm of approximation theory for design of MLP's are taken into consideration while designing analog activation functions [132, 133]. Theanalyses of the activation functions in generalized Multi Layer Perceprtrons (MLPs) that followsback propagation (BP)algorithm for the neurons of hidden and output layers improves overall performance of the Neural Network[24, 25, 129, 134].

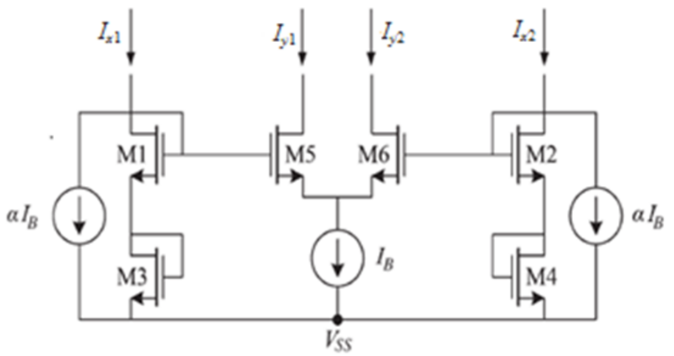

Figure.3. Current mode weak inversion f(x, n) implementation in CMOS[137]

4.1 Activation functions and derivatives

For experimental comparisons, conventional differentiable and monotonic activation functions like Sigmoid and Hyperbolic tangent function have been analyzed and used for MLP architecture [129, 132, 133, 135, 139, 140].The output for various current values in case of current mode circuit maybe observed[141]. The use of CMOS circuits to design sigmoid circuit can be observed as there is already literature that supports asynchronous voltage mode circuits that uses pulse stream technique [32, 33, 142, 143].

With reference to topologies viz., the Hyperbolic Tangent Approximation Circuit (HTAC), and the Advanced Hyperbolic Tangent Approximation Circuit (AHTAC) analyses using the general translinear principle shows that the activation function is being affected by the body effect but the derivative function has high immunity[136, 137].The design of non-linearneural activation function can be approximated accurately to tanh*(nx)* functionwith circuits like*hyperbolic tangent predistortion circuit (*HTPC*s*) and the *hyperbolic tangent slope multiplier circuit of order n (*HTSMC*n*)[138].

Table II shows example of specific parameter results and the plots have been observed to corroborate the theoretical approximations that are quite suitable for accurate analog implementation of the hyperbolic tangent function. Derived mathematically from Padé Rational approximation that can give better approximation to origin is given by

$$f_n(x) = \frac{3nx}{3+n^2x^2} \quad (7)$$

where n is the slope of this function at x=0 where the accuracy improves with n<1.

TABLE II PARAMETERS IN VARIOUS ANALYSES OF CURRENT MODE TRANSLINEAR ACTIVATION FUNCTION CIRCUITS IN SUBTHRESHOLD REGION

Paper	Type of Activation function V	Supply voltage V	Slope values	Power Dissipation µW	Bias Current I_b	Technology and tool used
[136]	*HTACs AHTACs*	1.15 1	0.6 to 1.1	1.1 to 0.42	I_b=100 nA	0.35µA Level 53 BSIM3v3.2 AMIS CMOS Technology Tanner Tools
[137]	*f(x, n) g(x)*	1.8 2.5	≥2	1.8 to 2.5 2.03 to 2.81	I_b=500 nA	0.35µA Level 53 BSIM3v3.2 AMIS CMOS Technology Tanner Tools

[138]	*HTPCs AHTP Cs*	1.14 0.96	0.6 to 1.1	1.09 to 0.42 0.58 to 0.28	I_b=100 nA	0.35µA Level 53 BSIM3v 3.2 AMIS CMOS Technology Tanner Tools

V = Volts, W= Watt, Hz = Hertz; A = Ampere

The accurate Hyperbolic Tangent approximation function has been hence been given

$$HTAF_n(x) = \frac{tanh(n)nx}{tanh(n) + (n - tanh(n))x^2} \quad (8)$$

The approximation to *tanh(nx)* carried by Eq.7 and Eq.9 has been simulated in MATLAB for various values of slope n[144].
In case of minimum size activation functions, a function *f(x, n)* that achieves properties with better convergence field is realized using CMOS circuits in Fig.3 and is given by

$$f(x,n) = \frac{4nx}{4+n^2x^2} \quad (9)$$

In Fig.3, the general TLP is followed for the design of *f(x, n)* in weak inversion region wherein $I_B$is the bias current, *Ix* and *Iy* are the signal currents, with I_{x1}, I_{x2}, I_{y1} and I_{y2} as input currents. To bypass difficulties in implementation of *f(x, n)*, another function *g(x)* is introduced and *g(f(x, n))* is given by

$$g(f(x,n)) = \frac{1}{2}\left(\frac{(4-n^2x^2)^2}{n^2x^2(4+n^2x^2)+16}\right) \quad (10)$$

f(x, n) is normalized to yield $\tilde{f}(x,n)$ to have a derivative with ½ its maximum value and is given by

$$\frac{\partial \tilde{f}(x,n)}{\partial x} = -\frac{2n^2x^2-8}{n^4x^4+8n^2x^2+16} \quad (11)$$

Algorithm 1. $\boldsymbol{x\ vs. \frac{\delta \tilde{f}(x,n)}{\delta x}\ and\ x\ vs.\ g(f(x,n))}$

Input: n varies from 2 to 16 in steps of 2
Input $f(\boldsymbol{x},\boldsymbol{n})$

Representations: x in x-axis with derivative plot on y-axis for even values of n

Output: Plots for $\frac{\delta \tilde{f}(x,n)}{\delta x}\ vs.\ \mathrm{g}(f(x,n))$ in same graph
for n=2:2:16

***Plot* 1:**

$$\tilde{\boldsymbol{f}}(\boldsymbol{x},\boldsymbol{n}) = \frac{\boldsymbol{f}(\boldsymbol{x},\boldsymbol{n})}{\boldsymbol{2n}} = \frac{\boldsymbol{2x}}{\boldsymbol{4+n^2x^2}}$$

Compute partial derivative $\boldsymbol{\delta \tilde{f}(x,n)/\delta x}$

Plotx vs$\frac{\partial \tilde{f}(x,n)}{\partial x}$at [-1, 1]

Plot 2:
Input computed $\mathbf{g}(\boldsymbol{f}(\boldsymbol{x},\boldsymbol{n}))$expression

Plotx vs$\mathbf{g}(\boldsymbol{f}(\boldsymbol{x},\boldsymbol{n}))$at [-1, 1]
End

The algorithm 1 described is an example followed for various plots and we obtained the results using MATLAB.
A unique mathematical condition that was satisfied using these derivatives are significant [137] and we found also:

$$\frac{\partial^2 f(x,n)}{\partial x^2}\Big|_{x=0} = \frac{\partial^2 \tilde{f}(x,n)}{\partial x^2}\Big|_{x=0} = 0 \text{ [144] } (12)$$

This design has been carried out with transistors working in the weak inversion region, using current mode techniques as well as fully differential and balanced topologies [138].The simulated results of these configurations have been presented for a range of slope values[138]. These simulations approximate suitably to accurate analog implementation of hyperbolic tangent functions[138, 145].

4.2 Analog Realization

More realizations of activation function have been analyzed.

- Asynchronous pulse stream neuron with sigmoid circuit for a pulse stream neural network is relevant; whose simulation result shows the neuron's communication to the sigmoid function [146].
- Another analog implementation of programmable sigmoid neural activation function and its derivative has been designed with bias currents to determine the upper and lower limits of the sigmoid, capable of working in the weak inversion region implemented in AMIS 0.35 µm technology [139].
- A digital hardware implementation of the hyperbolic tangent sigmoid function that does VLSI implementation using 0.18μm TSMC CMOS process has been presented and the design considers area × delay as a measure of performance and this parameter is quite important in our design methodology with pulses[145].
- A NMOS/PMOS design for sigmoid function as the activation function has been realized biased using one biasing voltage with the regions of operation are triode and saturation regions in 90-nm CMOS technology, this work can be extended to be observed in weak inversion region as well[140].

5. Analog Neural Network

As our survey focuses on analog neural network as a whole, other than addressing sub-circuits to make up the design like Multiplier and Activation function, it is necessary to survey the existing CMOS analog neural networks and their performance. Our design methodology survey is done in such a way so as to focus on current mode low power neural systems [44, 128, 12, 147, 148]. The current mode approach allows the designer to overcome difficulties arising from the parametric variability in CMOS devices that operate in the subthreshold region and provides reasonable solutions for circuit problems [41, 85, 149]. It describes a set of analog MOS circuits conceived for the design of analog VLSI neural systems that uses translinear principle [57, 60, 69, 70, 150, 151]. As previously noticed in this survey, the particular choice of the subthreshold region of operation is justified by advantages like high integration density and low power [22, 41, 42]. It is apparent that subthreshold analogelectronics offers striking means for implementation of massively parallel processing systems in which low power consumption is the basic need.Here, we present the survey on neural network, built using the subcircuits previously described.

The synthesis of CMOS subthreshold building blocks for the design of analog neural systems in current mode using translinear subthreshold MOS circuits have been used to obtain a robust design and low power dissipation[84]. The transistors are considered to have the same size to ensure density in the circuits and the simulations performed have been carried out using ANALOG tool 2μm CMOS process [84, 85].

Analog VLSI circuit techniques has been proven to offer area-efficient implementation of the functions required in a neural network such as multiplication, summation and sigmoid transfer function[21, 152]. Here, the architecture has been shown to be well suited for BP and weight perturbation algorithms with voltage resistors to make up the multiplier part [152]. The solutions to the problems in the design of ANNs like accuracy, precision, memory retention rate, and device mismatch is significant here [152].

Analog neural network synthesis system with synapse and neuron circuitry has been modeled that shows difficulties with model mismatches and performance degradation in function approximation applications [153]. The neural network has been partitioned for simulation using SPICE [153].

A power economic CMOS neuron can be designed with number of synapses, such that currents provided by the synapses can be easily summed in a single node at the neuron input [154]. Compatibility between neuron and synapses have been investigated simulated using SPICE with performance measurements done using a chip fabricated in a 0.35 μm CMOS process[154].

Epsilon chip, a large-scale generic building block device designed by Edinburgh University with large number of synapses and neuronal circuits is of profound significance for our design as it employs pulse stream technique [155; 15]. We notice pulse stream technique being focused on Image and Vision applications [15, 36, 155, 156].

Another work more appropriate to our survey was the analog design based on current mode translinear techniques using MOS transistors working in the weak inversion region [134].This design has been implemented for on-chip BP learning algorithm based on MLP. The main circuit topologies of synapses and neurons have been designed based on both current mode techniques and fully-differential configurations [134]. The blocks include simple cells, viz., the multipliers, activation functions, derivatives, and weight update circuits[136, 137, 138]. The circuit called Analogue Neural Net, has been prototyped on CMOS AMIS 0.5μm technology with two versions of MLPs 2-1 and 2-2-1 implementations supply voltages from 2.5V to 1.8V[134].

There have been profound contributions in various literatures available that confines us to discuss on ANN to the relevant criteria of subthreshold, translinear analog circuits and pulse stream techniques[30, 39, 46, 49, 80, 104, 157, 158, 159, 161, 162, 163, 164, 165, 166, 167, 168]. These have to be used in unification to achieve reasonable parametric design.

6. CONCLUSION

The review presents circuits that can provide VLSI building blocks for the development of current mode translinear subthreshold CMOS circuits that can be used to obtain optimal design of pulsed ANN. Subthreshold analog electronics offers means of implementing large scale distributed processing systems and wide use in communication systems and biomedical applications like retinal and vision chips. We propose to design the ANN with relevant CMOS sub circuits using 0.18μm technology with CADENCE SPECTRE tool.

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Ayyavoo Mithila is a Research scholar in the Department of Electronics and Communication Engineering, Sri Krishna College of Technology, Coimbatore. Her areas of interest include Analog VLSI Design and Neural Networks.

Vijayakumari Valsalam completed her B.E., (ECE) in 1993 and her M.E., Applied Electronics in 2005. She completed her PhD in Anna University, Chennai in 2011 and has published more than 30 papers in International journals and conferences. Her fields of interest include Image processing, Wireless sensor networks, Electronic circuits and Analog VLSI Design.