International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 11 (2015) pp. 27683-27694
© Research India Publications
http://www.ripublication.com

Test Vector Based Multiple Parametric Faults Detection In Non Linear Analog Circuits

G.Puvaneswari[1] , S.UmaMaheswari[2]
[1]Department of Electronics and Communication Engineering, Coimbatore Institute of Technology, Coimbatore-641014, India
E-mail: puvana1977@gmail.com (corresponding author)
[2]Department of Electronics and Communication Engineering ,Coimbatore Institute of Technology, Coimbatore-641014, India

Abstract

A method for multiple parametric fault diagnosis in non linear analog electronic circuits using test vector approach is proposed in this paper. The circuit under test (CUT) is simulated using Modified Nodal Analysis (MNA) and tested under DC condition. The test vectors corresponding to all the elements of the fault free circuit are found with the knowledge of circuit component values and topology. As the test vectors are found to be the function of circuit component values, the tolerance limits of the circuit components affects the practical implementation of the proposed approach in real time testing. To solve this issue, the test vectors are generated for upper and lower bound values of the components of CUT and testing is performed. Effectiveness of the proposed approach in locating multiple faults in nonlinear analog circuits is validated through simulation results of benchmark circuits.

Keywords: non linear analog circuits – modified nodal analysis- test vector – fault diagnosis

Introduction

Analog circuit testing aims to locate parametric faults called soft faults and catastrophic faults called hard faults. Soft or parametric faults are due to variation in circuit component values where as hard faults are due to open or short circuits. Most of the research works are towards parametric faults detection because they are hard to find and leads to variation in overall system performance, not complete variation as due to hard faults. And also the factors like nonlinearity of circuit components, tolerance and the number of test nodes to locate the faulty elements, limit the development of standardized methods and models for testing. Different methods have been proposed to detect single and multiple faults in nonlinear analog circuits. In [1],

a complex field modeling method is proposed to identify both hard and soft faults and to solve tolerance issue. In [2], single soft fault detection approach using multiple objective optimization method is proposed. A two stage algorithm to locate multiple faults in nonlinear analog circuits is proposed in [4]. In the first stage for different DC voltages applied to accessible nodes, the measurements are made to form the test equation. The test equation is linearized by Taylor series expansion. The rank of the matrix with derivatives of the function describing the system is first found and an integer is chosen for single and multiple faults to form the sub matrices of the matrix and solved by the method of normal equation. The accuracy of the solution is improved by Newton-Raphson approach. In the second stage the faulty components are located from the solution vectors. A method for finding the DC operating points of transistor circuits is proposed in [5]. The DC behavior of the CUT is described by systems of nonlinear algebraic equation. To obtain multiple DC operating points Homotopy method is used. A method for multiple soft fault diagnosis of nonlinear static circuits is proposed in [6]. The approach uses Homotopy approach for finding multiple DC operating points of the CUT. From multiple solutions the correct solution is found based on some physical constraints such as negative resistance. In [7], wavelet transform coefficients of the supply current and the output voltage are found. Then, distance measure is found for the faulty and fault free CUT. Then the CUT is declared as faulty if this measure for faulty CUT is greater than the measure for the fault free circuit. An efficient and totally feasible algorithm intended to the time-domain analysis of nonlinear lumped analog circuits was developed and implemented in a computation program [8]. It overcomes some restrictions of the modified nodal approaches, having practically an unlimited degree of generality.

In [3], a method to detect single fault using testability vectors in linear analog circuits is proposed. The CUT is simulated using modified nodal analysis and the equations are solved using the linear system solver with Lower and Upper Triangular Decomposition. Testability vectors are found for all the circuit components. The testability vectors form the fault dictionary to diagnose the faults in the CUT. The tool calculates the fault variable for each test frequency and finds the average, standard deviation and coefficient of variation of the real and imaginary parts of the elements. The sum of the cumulative coefficients of variation for each element is calculated and the lowest one indicates the diagnosed faulty element. The proposed work is based on the test vectors as in [3] but proposes solution to solve challenges in real time testing and for multiple soft faults detection in analog circuits with nonlinear devices such as diodes and transistors.

In the following sections, detailed procedure to detect multiple faults has been explained. Section 2 describes the mathematical fundamentals of the proposed approach for nonlinear circuit testing. Section 3 illustrates the test procedure and describes the challenges in real time testing and the proposed solution. Section 4 deals with the results obtained from the proposed work on the bench mark circuits. Section 5 is about the discussion regarding the proposed approach & section 6 concludes the proposed work.

Mathematical Fundamentals

The analog circuit test procedure begins with the simulation of the CUT and deriving the diagnosis variables such as node voltages and branch currents. The simulation of an electronic circuit involves formulation of the circuit equation and solving it for the unknowns. To simulate the CUT, Modified Nodal Analysis (MNA) is used. MNA uses the voltage, current relationship of the circuit components and the KCL [9, 10]. It handles voltage sources effectively by an unknown current through it and adds it to the vector containing unknown node voltages. MNA for linear systems results in the system equation of the form

$$AX = Z \tag{1}$$

where A is the coefficient matrix, X is the unknown vector consists of circuit variables (node voltages and few branch currents) and Z is the excitation matrix. The circuit coefficient matrix is formed by the sub matrices,

$$A = \begin{bmatrix} G & B \\ C & D \end{bmatrix} \tag{2}$$

G is the conductance of the components in the CUT and the values of G are determined by the interconnections of the circuit components. B and C matrices consist of 0, 1,-1 and the values are based on the interconnections of the voltage sources. The D matrix is developed with zeros for independent sources and has nonzero values for dependent sources. The X matrix with variables useful for the diagnosis is formed by the node voltages and the unknown currents through the sources.

$$X = \begin{bmatrix} V_n \\ I_v \end{bmatrix} \tag{3}$$

The right hand side matrix (Z) consists of the values of independent current and voltage sources.

$$Z = \begin{bmatrix} I \\ V \end{bmatrix} \tag{4}$$

The unknown vector is found by solving the linear system equations. In case of circuits with nonlinear devices, the nonlinear devices are modeled using their large signal or DC models [12]. The current through the devices is introduced as a new circuit variable in the unknown vector. The circuit equations obtained from MNA are solved using Newton Raphson (NR) method. To reduce the iteration dependent blocks [12] the nonlinear device equations are arranged as from (5) to (9) and the circuit matrix is formed as in (10). The nonlinear devices are described by their V-I relationship as

$$V = f(I) \tag{5}$$

The Taylor series approximation (neglecting higher order terms) of (5) is,

$$V^{K+1} = V^K + (df(I)/dI)^K (I^{K+1} - I^K) \tag{6}$$

Where K- NR iteration number,
Rearranging (6),

$$V^{K+1} - (df(I)/dI)^K I^{K+1} = V^K - (df(I)/dI)^K I^K \tag{7}$$

Let $V^K - (df(I)/dI)I^K = a^K$ (8)

Now (7) becomes

$$V^{K+1} - (df(I)/dI)^K I^{K+1} = a^K \tag{9}$$

$$\begin{bmatrix} G_{11} & . & . & G_{1n} & B_{11} \\ . & . & . & . & . \\ . & . & . & . & . \\ G_{n1} & . & . & G_{nn} & B_{n1} \\ C_{11} & . & . & C_{1n} & -(df(I)/dI)^K \end{bmatrix} \begin{bmatrix} V_1^{K+1} \\ . \\ . \\ . \\ I^{K+1} \end{bmatrix} = \begin{bmatrix} . \\ . \\ . \\ . \\ a^K \end{bmatrix} \tag{10}$$

Faults in the CUT are simulated using Fault Rubber Stamp (FRS) [3,12]. FRS is based on the MNA stamp of the components of a CUT. The MNA stamp of a component C_n connected in between the nodes j and j' (V_j , V_j'- respective node voltages) ,in the coefficient matrix is,

$$\begin{array}{c} \\ j \\ j' \end{array} \begin{array}{c} \begin{array}{cc} V_j & V_j' \end{array} \\ \begin{bmatrix} +C_n & -C_n \\ -C_n & +C_n \end{bmatrix} \end{array} \tag{11}$$

If this component is assumed to be faulty, its value changes from C_n to $C_n \pm \Delta$. This deviation causes the current through that faulty component to deviate from its nominal value. This current deviation called fault variable (ϕ) is introduced in the faulty circuit unknown matrix as an unknown branch current. To indicate the current deviation through the faulty component, the faulty component is represented as a parallel combination of its nominal value and the deviation (Δ) (fig.1). V_j and V_j' are the node voltages at the nodes j and j' respectively. i_f is the current deviation through the faulty component.

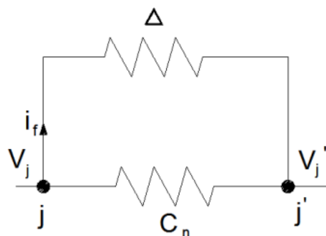

Figure 1: Faulty Component Representation

The fault rubber stamp [3, 12] for the component C_n is,

$$\begin{array}{c} \\ j \\ j' \\ \\ f \end{array}\begin{array}{c} \begin{array}{cccc} \boldsymbol{V_j} & \boldsymbol{V_j}' & & \boldsymbol{i_f} \end{array} \\ \left[\begin{array}{ccc|c} +C_n & -C_n & \vdots & 1 \\ -C_n & +C_n & \vdots & -1 \\ \cdots & \cdots & \cdots & \cdots \\ \hline 1 & -1 & \vdots & -\Delta^{-1} \end{array}\right] \end{array} \tag{12}$$

The bottom row line is the faulty component equation and the right most column corresponds to the extra fault variable. As seen in (12), for each faulty component there is an additional column at the right side and row at the bottom of the coefficient matrix is introduced. The faulty system with the FRS in matrix form is,

$$\begin{bmatrix} A & c \\ r & \Delta \end{bmatrix} \begin{bmatrix} X_f \\ \phi \end{bmatrix} = \begin{bmatrix} Z \\ 0 \end{bmatrix} \tag{13}$$

where c and r are the additional column and row introduced corresponding to a faulty component. The additional column c indicates the location of the faulty component. The additional row r is the faulty component equation with its node voltages. The value of Δ depends on the faulty value of the component. It can be observed that a new variable called fault variable (ϕ) is also introduced as unknown into the unknown vector matrix (X_f) of the faulty circuit. It can also be noted that this fault variable is the unknown branch current. As seen in (13), the coefficient matrix (A) of the nominal circuit is retained in forming the faulty system equation without any modification in the values of it. Thus from (13), the faulty circuit equations are written as,

$$AX_f + c\phi = Z \tag{14}$$

$$rX_f + \Delta\phi = 0 \tag{15}$$

replacing $Z = AX$ from (1),

$$AX_f + c\phi = AX \tag{16}$$

$$A(X - X_f) = c\phi \tag{17}$$

$$X - X_f = A^{-1}c\phi \tag{18}$$

$$X - X_f = t\phi \tag{19}$$

$$\phi = (X - X_f)/t \tag{20}$$

$$t = A^{-1}c \tag{21}$$

The product $A^{-1}c$ is a column vector and it is called testability vector [12]. As c describes the location of a component in the CUT, the testability vector is associated to that component and the values are independent of the faults. Thus the fault variable which can be obtained by the element wise division of the difference vector (difference between the nominal and the faulty solutions) and the testability vector is also associated to a specific component in the CUT and the rows are associated to the diagnosis variables or the circuit variables [12].

Test Procedure

The test process shown in flow diagram (fig.2 &3), begins with the development of test vector and then the diagnosis. The test vectors for all the components in the CUT are obtained by using (14-21). The CUT with the nominal component values is simulated and the solution vector (X) is obtained. Faults with different values are injected into the CUT and the solution vector (X_f) is found. The fault variable ϕ is obtained from (20) and found to have same column value for the faulty element. But it can be observed from (18, 19), the test vectors are the function of component values. In real time testing, the component values are not with the nominal values and are within the tolerance limits. Therefore the column values are not the same for faulty elements and fault detection process fails. To solve this issue, the proposed approach generates test vectors for upper and lower bound limits of the components of CUT with the assumption that the circuit topology and the component values with tolerance limits are known. Testing is done with maximum of two circuit variables and the nodes are input and output nodes (assuming that the nodes are accessible)

Real time test process involves two stages. In the first stage called pretesting stage, the test vectors are generated for upper and lower limits of components values. The circuit variables are obtained by solving the MNA equations with the nominal, upper and lower bound circuit component values and stored. The CUT is said to be fault free only when the circuit variables measured at the test nodes are within the bound values. In the second stage called test stage, faults are injected into the CUT and measurements are made at the selected nodes. The fault variable is found from (20) with upper and lower bound test vectors. The relative standard deviation related to the mean of each column (associated with the components in CUT) is found. The mean value of relative standard deviation of all the columns is found and has been set as a threshold for the detection of faulty elements. An element of the CUT is said to be faulty when the estimated relative standard deviation is lesser than the threshold found. The detailed algorithm is shown in fig. 2 & 3.

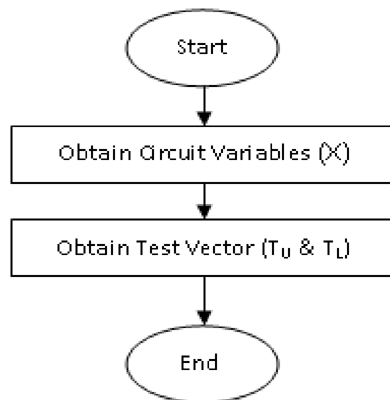

Figure 2: Pre testing stage

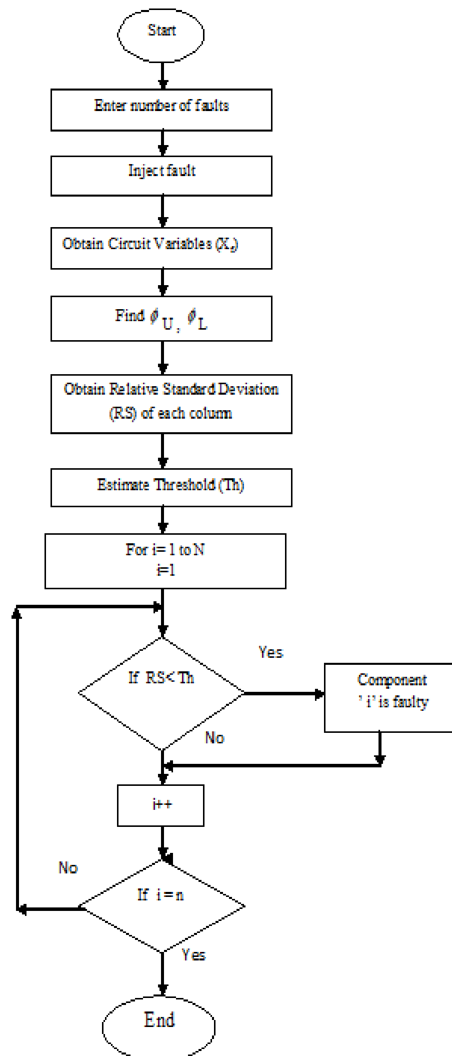

Figure 3: Testing Stage

Ambiguity Set Determination
The ambiguity sets are determined as in [3, 12]. Two or more circuit components belong to same ambiguity set if a fault cannot be resolved between them. Ambiguity sets can be located with test vectors. Two elements belong to same ambiguity group if and only if their test vectors are equal.

Illustrations
The efficiency of the proposed work is validated through benchmark circuits like Diode circuit, Transistor amplifier circuits at DC condition.

Diode Circuit
The CUT with its nominal value is shown in fig. 4. The diode is modeled using exponential models [11]. A current of 1A is applied at node 1.The circuit equations are assembled using MNA as mentioned above. A column vector (c) corresponding to the location of each component is derived and the test vector as in (19) is calculated for all the components with upper and lower bound values (fig.5 &6) respectively. Multiple faults of different magnitudes are injected into the CUT and the faulty circuit is simulated. The fault variable is found. Fault diagnosis is performed as explained in the flow diagram. Testing is done with the diagnosis variables (node voltages) measured at test nodes 2 & 5.

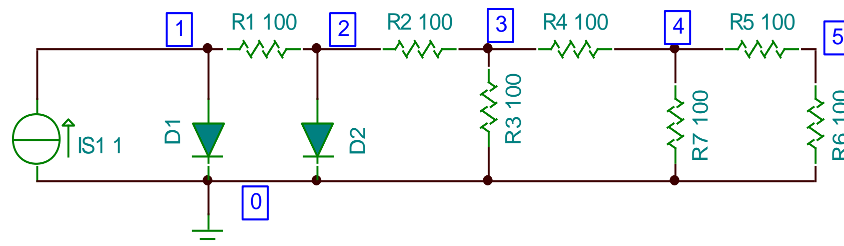

Figure 4: Diode Circuit

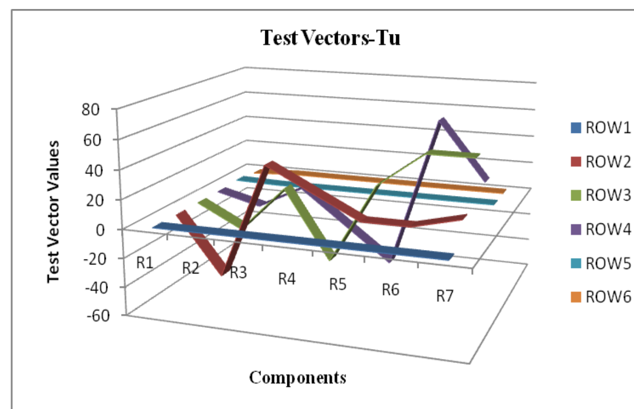

Figure 5: Test Vectors (Diode Circuit)

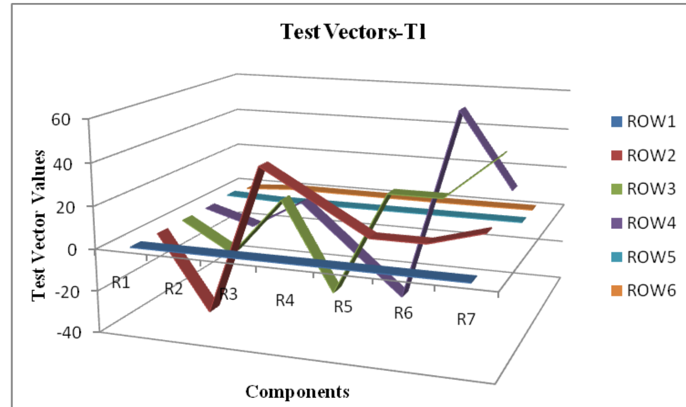

Figure 6: Test Vectors (Diode Circuit)

Two Fault Case

Two faulty components R_1 & R_2 with the component values 110Ω, 80Ω are injected in to the CUT. Fault detection is performed as explained in fig. 3. The column relative standard deviation values obtained are 1.15, 0.2, 1.99, 1.99, 1.99, 1.99, 1.99 (corresponding to seven circuit components). The mean (threshold) value from these values is 1.62. The column with lesser than this threshold value is declared as faulty. Therefore components R_1 & R_2 are declared as faulty. The values for other faulty conditions are listed in Table 1.

Table 1: Results For Different Fault Conditions

CUT	Faulty Component & Value	Threshold	Relative Standard Deviation obtained for faulty components
Diode circuit	R_3 (200 Ω) R_4 (50 Ω)	0.79	0.129 0.0177
	R_1 (250 Ω) R_3 (115 Ω) R_5(60 Ω)	0.749	0.09 0.453 0.04
	R_1 (55 Ω) R_5 (155 Ω) R_7 (112 Ω)	0.701	0.0577 0.115 0.115
	R_1 (40 Ω) R_2 (75 Ω) R_3 (150 Ω) R_4 (180 Ω)	0.672	0.0577 0.64 0.428 0.115

Transistor Circuit

The transistor circuit under test is shown in fig.7. Transistors are replaced by their equivalent DC models with the model parameters β=100, base-emitter saturation current 17.9fA & base -collector saturation current 17.9fA. Fault detection is performed as in fig. 3. The test vectors are shown in fig. 8 & 9 for the upper and lower

bound values of the components of CUT respectively. It is observed that the test vectors are found to be same for both R_2 and R_3. Therefore as explained in 3.1, the faulty conditions of these two elements are hard to find.

Two fault case

Two faulty components R_1 & R_4 with values 1500Ω, 800Ω are injected into the CUT. The relative standard deviation of each column (four columns corresponding to four components of CUT) is found to be -4.29, 0.374, -0.374, -2 and the threshold value is obtained as -1.57. Therefore the element with relative standard deviation value lesser than this is declared as faulty. Hence R_1 & R_4 are found to be as faulty.

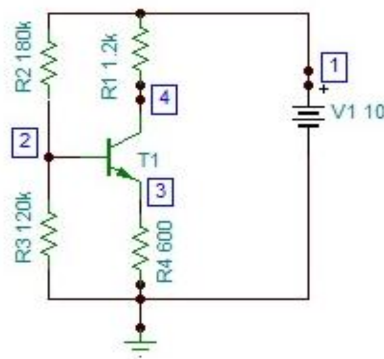

Figure 7: Transistor circuit

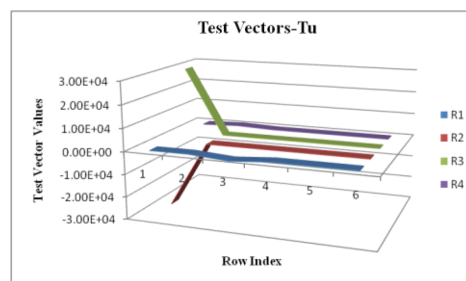

Figure 8: Test Vectors (Transistor circuit)

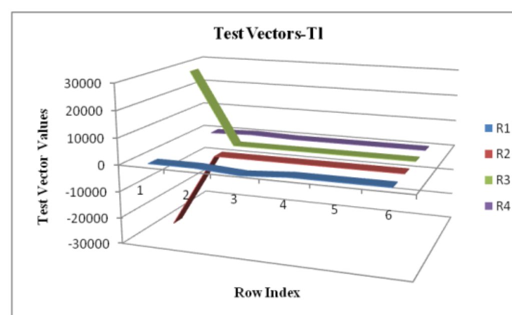

Figure 9: Test Vectors (Transistor Circuit)

Three fault case

Three faulty components R_1,R_2 & R_4 with values 1500Ω, 80Ω, 50Ω are injected as faulty into the CUT. The relative standard deviation obtained is -4.94, 2.28, -2.28, 3.39. The threshold obtained from these values is -0.387. The relative standard deviation value lesser than this corresponds to R_1 (first column), R_3 (third column). Therefore the fault diagnosis is not successful because of R_2 & R_3 test vectors. To solve this, in real time testing the current flowing through these elements can be measured to diagnose faulty conditions. The elements that form ambiguity set can be identified while obtaining the test vectors itself (pre testing stage). This necessitates the additional measurement of current to diagnose the faulty condition.

Discussion

A test approach to detect multiple faults using test vectors is proposed. The approach uses MNA to simulate the CUT. The algorithm checks for the columns of the fault variable with the relative standard deviation value lesser than the threshold to identify faulty components. In real time testing, the component values cannot be with the nominal values and be within the tolerance limits. This limits the fault detection procedure which is performed by the test vectors generated with component nominal values. To solve this issue, test vectors are generated for lower and upper bound values of the components of CUT and testing is performed. With the obtained test vectors, it is also possible to identify the components that cannot be identified under faulty conditions. It can also be observed that the testing can be performed with few circuit or diagnosis variables.

Conclusion

A method for locating multiple faults in nonlinear analog circuits is proposed. The approach is based on the test vector of the components of the CUT. The test vectors are derived from the coefficient matrix and the location of the components in the CUT. A mean value based threshold technique is adapted to locate multiple faults in the CUT. Results are shown up to four faults condition because of the threshold value chosen.

References

[1] Y. Gao, C. L. Yang, S. L. Tian, "Methods of Handling the Aliasing and Tolerance Problem for a New Unified Fault Modeling Technique in Analog-Circuit Fault Diagnosis", Advanced Materials Research, Jul. 2014,Vol 981, pp. 11-16.

[2] Zhou Longfu, Hu Yonghe, Zhang Chaoqun, Li Zheng, " The application of multi-objective programming in single soft-fault diagnosis of nonlinear analog circuit with tolerance", IEEE 11th International conference on

Electronic Measurement & Instruments, 16-19 Aug. 2013, Vol.2 , pp.829-832.

[3] Jose A.Soares Augusto and Carlos Beltran Almeida, “A Tool for Single-Fault Diagnosis in Linear Analog Circuits with Tolerance Using the T-vector Approach”, Hindawi Publishing Corporation, VLSI design, 2008, pp 1-8.

[4] M. Tadeusiewicz, S. Halgas, “Multiple soft fault diagnosis of nonlinear DC circuits considering component tolerances”, Meterology & Measurement Systems, 2011, Vol. XVIII, 3, pp.349-360.

[5] Ljiljana Trajkovic, “DC operating points of transistor circuits, Nonlinear Theory and Its Applications”, IEICE, 2012, vol.3, no.3, pp 287-300.

[6] Michal Tadeusiewicz, Stainislaw Halgas, “Multiple Soft Fault Diagnosis of Nonlinear Circuits using Continuation method”, J Electronic Testing: Theory and Applications ,2012, DOI 10.1007/s10836-012-5306-3J.

[7] JAlexios D. Spyronasios, Michael G. Dimopoulos, and Alkis A. Hatzopoulos, “Wavelet Analysis for the detection of Parametric and Catastrophic faults in mixed signal circuits”, IEEE Transactions on Instrumentation and Measurement, 2011, vol.60, no.6, pp 2025-2038.

[8] Lucian Mandache, Dumitru Topan, Ioana-Gabriela Sirbu, “Improved Modified Nodal Analysis of Nonlinear Analog Circuits in the Time Domain”, Proceedings of the World Congress on Engineering, Vol II, WCE 2010, London, UK.

[9] C.-W. Ho, A. Ruehli and P. Brennan, “The modified nodal approach to network analysis”, IEEE Transactions on Circuits and Systems, 1975, Vol.22, no.6, pp.504-509.

[10] Jiri Vilach and Kishore Singhal, Computer methods for circuit analysis and design, Van Nostrand Reinhold Company, 1983.

[11] Adel S. Sedra, Kenneth Carless Smith, Microelectronic Circuits, Oxford University Press, 2004.

[12] J. S. Augusto, C. B. Almeida, "FASTNR: An Efficient Fault Simulator for Linear and Nonlinear Circuits" VLSI'99 ("VLSI: Systems on a Chip", Kluwer), Lisboa, Portugal, 1999.