Global Journal of Pure and Applied Mathematics.
ISSN 0973-1768 Volume 12, Number 1 (2016), pp. 1077-1084

http://www.ripublication.com

Content Addressable Memory performance Analysis using NAND Structure FinFET

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Abstract

In the recent past, scaling in Complementary metal-oxide semiconductor (CMOS) technology has faced a bout of challenges such as the decrease in gate control, high power densities and sensitivity to process variations, and short-channel effects. On the other hand, Fin-type field-effect (FinFET) devices, also called as "multi-gate" transistors, have proved to produce better electrostatic control of the channel and have robust electrical characteristics such as faster switching off and on (of the device). FinFET is also known for its meticulous design with a thin vertical fin, wrapped and controlled by the gate from three sides. This paper proposes an effective design for the Content Addressable Memory (CAM) with NAND and NOR cell structure using the FinFET Technology, thereby largely reducing the issue of increased power consumption. This paper also covers a thorough performance comparison of NOR type CAM bit-cell with the NAND type CAM bit-cell using FinFET technology. The number of transistors used in the NAND type CAM bit-cell is less compared to NOR type CAM bit-cell.

Keywords: Content Addressable Memory (CAM), FinFET, NAND bit cell, NOR bit cell, low power.

1. Introduction

As per Moore's law, the number of transistors should double every month. In order to achieve that, the size of the transistors should be reduced in size to accommodate double the number per unit area.

But, when the device channel length is scaled down, the short channel effects are increased. FinFET, known as an efficient technology, manages this shortfall. FinFET largely reduces the short channel effects of the devices with a good electrostatic control over the channel. VLSI (Very-Large-Scale Integration) designers mainly aim to meet the required performance with constraints like power (power efficiency) and area (the size). As the name suggests, FinFET comprises fins that form the source, utilizing a portion of the transistor, and providing the path in the channel for the current to flow when it is switched on. The gate that controls the switching operation covers the fins to form a 3-D structure. In a device structure like this, the fin body requires to be depleted completely even in the sub-threshold region. This leads to good electrostatic control of the channel, resulting in better electrical characteristics, such as quick turning on and off. Practically, fin body is required for the wrapped gate to have good control over the channel.

FinFET, which is a double-gate device, is the best option for bulk CMOS at the nano scale. FinFET uses the Back Gate to control the threshold voltage (VT) of the front gate, which is an important parameter of the device. This helps in improving the circuits in delay, area and power. As per the proposed design based on complete analysis, the CAM is designed in Short Gate (SG) FinFET technology to achieve minimum delay in SG mode.

Two more challenges arise from this – reducing the leakage current (sub-threshold gate leakage), and reducing yield device to device variability. FinFET is a good solution to manage the challenges, and also chosen as a more adaptable option for Fabrication than CMOS. CAM is known as better computer memory used for many high speed searching applications. In standard memory, data search is addressed by Memory address of an input data. However, in the existing CAM, NOR type CAM bit-cell is used. In case of basic CAM Architecture, NOR type CAM bit-cell design consumes more power because it requires more transistors compared to NAND type CAM bit-cell. Increased power consumption is a result of its high searching speed. CAM consists of two types of forms: Binary CAM and Ternary CAM. Binary CAM searches for the binary data bits zeros (0's) and ones (1's) and also stores it. Ternary CAM searches and stores data bits zeros (0's), ones (1's) and excludes (X). CAM design mainly aims to reduce power consumption associated with the large amount of parallel active circuitry, without compromising on memory density and speed. CAM is ideally used in applications where instant data search is required. For example, ATM switches, routers and processors. It parallel searches the input data with a single clock cycle, leading to high power consumption. Not only is its searching speed high, but power consumption is equally high.

2. Design of CAM cell using FinFET Technology

2. 1 CAM cell

The CAM cell depends on the static memory cell and in cross-coupled inverters, the data is stored in SRAM. While the two NMOS transistors are controlled by the word line and allow CAM to write the data, the remaining transistors are used in CAM to match the input and stored data. Static RAM has two transistors used to store the bit

for searching. This cell performs browse operation in addition to write operation just like the SRAM cell. The other is match operation.
CAM can be divided into NOR, NAND, and ternary categories, based on the different designs of core memory cells and matching circuits. The core memory cell, particularly a 6T SRAM cell, is used for data storage; the XOR/XNOR matching circuitries used for comparing data are the components of CAM bit-cell.

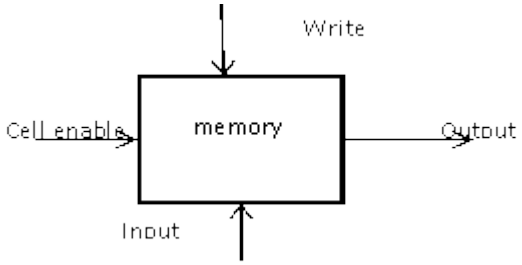

Fig 2. 1: Basics CAM Cell

2. 2 Components of CAM cell
A CAM bit-cell consists of a core memory cell that includes 6T SRAM cell used for storing data, and the XOR/XNOR matching circuitry used for comparing data.

2. 2. 1 SRAM Cell
A basic SRAM cell is made of six MOSFET transistors and every bit in an SRAM is stored on four transistors (PL, PR, NL, NR). These four transistors form two cross-coupled inverters. This storage cell has two states used to refer 0's and 1's. Two additional transistors are used to control the access to a storage cell during operations such as read and write in a six-transistor (6T) SRAM. A SRAM cell consists of three different states - standby mode which indicates that the circuit is in idle condition, reading mode indicates that data has been requested and writing mode indicates that content is being updating. The SRAM should have readability and write stability while operating in read and write modes.

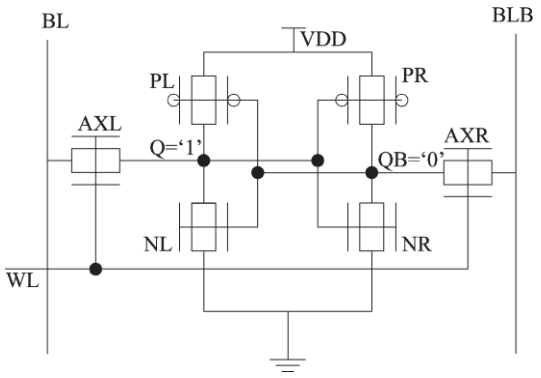

Figure 2.2: Six transistors SRAM cell using FinFET

2. 2. 2 XOR/XNOR matching circuitry

The XOR/XNOR matching circuitry is based on two kinds of digital logic gates, which are not basic gates in nature and constructed by combining both together. The output of a few more logic gates is Boolean function and considered as complete logic gates. These two logic gates are called the Exclusive – NOR (Ex- NOR) Gate and its complement form is the Exclusive –OR (Ex-OR) Gate. The matching circuits work based on the XOR or XNOR operation.

Table 2.1: Ex-NOR Gate Truth Table

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

Table 2.2: Ex-OR Gate Truth Table

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

2.3 NAND CAM bit cell operation

Logically, “1” on node B switches the M1 transistor ON. In the other match case, when SL=0 and D=0 the M1 transistor should be ON and it should be noted. During this case, the transistor M_D passes logic high to raise node B. In other cases in NAND, SL≠D result in discrepancy and node B will be of logic “0” and the transistor M_1 is switched to OFF. Transistor in node B implements the XNOR/XOR operation. The NAND nature of this cell is clear when multiple NAND cells are connected in series.

The ML_n and ML_{n+1} node are joined to form a word during this condition. A continuous chain of nMOS of all the M1 transistors is similar to the pull-down path of a CMOS NAND logic gate structure. This match condition takes place only when every cell in a word is in the match condition for the entire word.

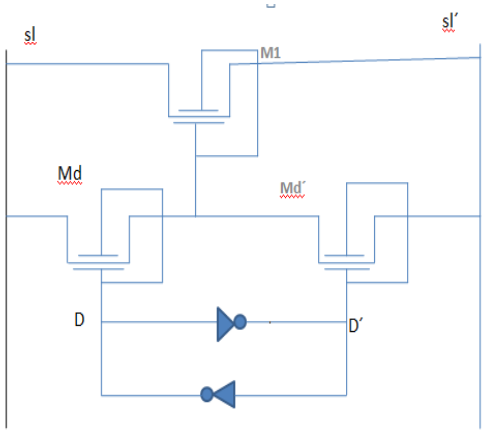

Figure 2.3: Schematic for NAND CAM bitcell

2.4 NOR CAM Bit cell Operation

The NOR cell compares the complementary stored bit D and $\overline{D}$and the complementary search data on the complementary search line, SL and SL_bar using four comparison transistors (T1 through T4), which are ideally minimum in size to maintain the high cell density. These transistors implement the pull down path of a dynamic XNOR logic gate with inputs SL and D. Each pair of transistors T1/T3 and T2/T4, forms a pulldown path from the matchline ML, in a way that a mismatch of SL and D will activate at least one of the pulldown paths connecting ML to ground. A match of SL and D disables both pull down paths disconnecting ML from ground. The NOR nature of this cell is evident when multiple cells are connected in parallel to form a CAM word by shortening the ML of each cell to the ML of adjacent cells. The pulldown paths connecting in parallel resembles the pulldown path of a CMOS NOR logic gate. A match condition on a given ML is possible only when every individual cell in the word has a match. In a NOR CAM bit-cell, transistors T1–T6 form the core SRAM cell, while transistors T7–T10 form the matching circuit.

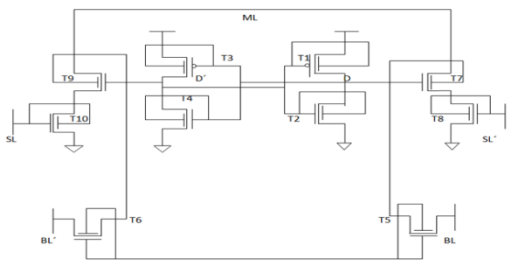

Figure 2.4: Schematic for NOR CAM bit cell

2.4 Static RAM Array

There are several techniques to improve SRAM cell performance and power; dynamic voltage scaling, lower retention voltage and the like. Most techniques, however, are not directly related to the CAM operation, and can be directly applied regardless of the selected CAM cell architecture. In view of the SRAM oriented techniques common to all CAM improvement methods, the report does not include SRAM optimization, rather a detailed study on CAM specific methods.

2.5 Match Lines (ML)

In a basic CAM design, the ML is precharged, and later evaluated to discharge or stay high based on the match or not match decision of the evaluation circuit. During the evaluation phase, the PRE signal is high and the search bits are loaded on bit lines. When two segments have match, then the match line discharges through any one of the pull-down paths. Constraints such as power, area, and delay in the ML routing limits the CAM array size and performance for many applications. This project suggests effective methods to reduce ML area, delay, and power.

2.6 Search Lines (SL)

The SL activity factor in a basic CAM design (which uses complementary search lines) is 1. This high activity factor shows that SL improvement techniques are best for minimizing the CAM power and delay. In this project, we present a way to avoid using complementary search lines, and reducing the activity factor to obtain area, power and delay benefits.

3. Result and Analysis

The following figures and power analysis shows the improved performance using NAND FinFET technic. The results are obtained for both NOR and NAND structures and compared.

3.1 NAND bit cell

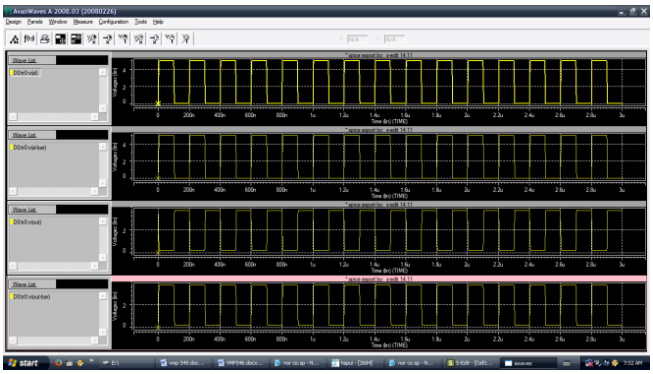

Figure 3.1: Output Waveform for Nandbitcell

Power Results

Search line

Average power consumed -> 1. 133459e-006W
Max power 1. 576689e-004W at time 2. 03557e-007
Min power 0. 000000e+000W at time 1. 05e-007

Match line

Average powerconsumed 2. 532900e-007W
Max power 1. 624798e-004W at time 3. 03552e-007
Min power 0. 000000e+000W at time 1. 05e-007

Delay Result

tdelay = -1. 0007e-007 s
Trigger = 3. 0450e-007s
Target = 2. 0443e-007 s

3.2 NOR bit cell

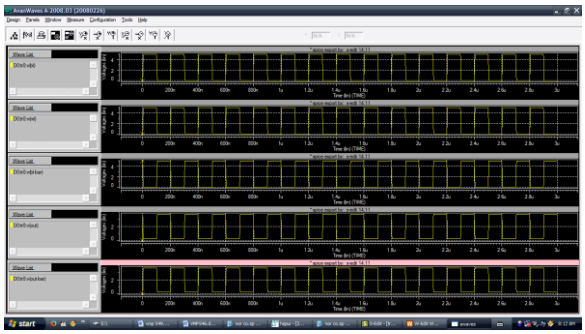

Figure 3.2: Output Waveform for Norbitcell

Power Results

Search line

Average power consumed1. 645729e-002 w
Max power 3. 345435e-002 W at time 5e-009
Min power 0. 000000e+000 W at time 1. 05e-007

Match line

Average power consumed 2. 869415e-002 W
Max power 5. 857086e-002 W at time 5. 1875e-007
Min power 0. 000000e+000 W at time 5e-009

Delay Results

tdelay = 1. 0025e-007 s
Trigger = 3. 0450e-007s
Target = 4. 0475e-007s

Conclusion

In conclusion, this paper discusses the advantages and prospects of designing the NAND CAM cell and NOR CAM cell using the FinFET technology. Minimizing power consumption is a key criteria, which is achieved by employing a delay in the CAM cell structure. The detailed power analysis reiterates that NAND CAM cell consumes less power than the NOR CAM cell and the delay is found to be1. 0025e-007(s). The HSPICE EDA tool is used to get the simulation results. The CAM cells act as amplifiers and compare the search data with the data stored in the memory; while NAND reduces the power consumption of the match-lines and search lines in CAM cell.

References

[1] K. Pagiamtzis and A. Sheikholeslami, "Content-addressable memory (CAM) circuits and architectures: A tutorial and survey, " *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 712–727, Mar. 2006.

[2] S. Hanzawa, T. Sakata, K. Kajigaya, R. Takemura, andT. Kawahara, "A large-scale and low-powerCAM architecture featuring a one-hot-spot block code for IP-address lookup in a network router, " *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 853–861, Apr. 2005.

[3] I. Arsovski and A. Sheikholeslami, "Amismatch- dependent power allocation technique for match-line sensing in content-addressable memories, " *IEEE J. Solid-State Circuits*, vol. 38, no. 11, pp. 1958–1966, Nov. 2003

[4] K. Pagiamtzis and A. Sheikholeslami, "A low-power content- addressable memory (CAM) using pipelined hierarchical search scheme, " *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1512–1519, Sep. 2004.

[5] A. Bansal, S. Mukhopadhyay, and K. Roy, "Device-optimization technique for robust and low-power FinFET SRAM design in nanoscale era, " *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1409–1419, Jun. 2007

[6] JencyRubia J, Gopal BG, Prabhu V, "Ananlysis, Design and implementation of 4 bit full adder using FinFET", Journal of Convergence Information Technolgy, Vol. 10, No. 2, Mar 2015 pp: 71-77