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Design and Implementation of Phase Locked Loop Using Current Starved Voltage Controlled Oscillator

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Abstract

This paper is based on CMOS Phase Locked Loop (PLL) using Current Starved Voltage controlled oscillator (CSVCO) in 180 nm process and describes the design and simulation of miscellaneous blocks of Phase Locked Loop (PLL) for the 6 GHz band. The reference frequency is 50 MHz and the Current Starved Voltage controlled oscillator output frequency is 1 GHz to 3 GHz in a state-of the-art 180nm process, with 1 V supply voltage. The design is implemented in Zeni Electronic Design Automation (EDA) environment tool with high oscillation frequency and low power consumption. Phase locked loop's were used in most of the application for clock generation and recovery as well. As the technology grows faster in the existing generation, there has to be quick development with the technique.

Keywords: CSVCO; PLL; Zeni□EDA; Oscillation frequency; power consumption.

1. Introduction

A PLL is a feedback system that compares the output frequency/phase with the input frequency/phase. Phase-locked loops can be utilized for frequency synthesizing, carrier synchronization, carrier recovery, frequency division, frequency multiplication and frequency demodulation [1]. A VCO is the heart of the PLL and can be designed either by LC or RC. A LC VCOs have superior phase noise performance compared with ring VCO'S. However, an LC VCO has a small tuning range large layout area and possibly higher power [2]. The ring oscillators, however, do not have the complication of the on-chip inductors required for the LC oscillators. Thus the chip area is reduced. In

addition to a wide tuning range; ring oscillators with even number of delay cells can produce quadrature-phase outputs. The phase noise performance of ring oscillators is much poorer in general [3], [4]. Also, at high oscillation frequencies, the power consumption of the ring oscillators may not be low which is a key requirement for battery operated devices [5]. To overcome these problems, we work on five stages current starved Oscillator and single stage source coupled oscillator without an LC tank. Finally their performances are compared based on their results.

A challenging work in the CMOS technology is to design a low phase noise ring oscillator for a Charge Pump Phase Locked Loop (CPPLL) using CMOS technology. A design presented here is to improve the overall characteristics of PLL. The first component of the PLL is the PFD which has been designed to improve the speed by minimizing the dead zone. The CP circuit improves the performance of the PLL because it has been designed for high bandwidth. The main part of this PLL is the CSVCO, which has been designed to get superior phase noise.

2. System Overview

Phase-locked loops (PLLs) generate well-timed on-chip clocks for various applications such as clock and data recovery, microprocessor clock generation and frequency synthesizer. The basic concept of phase locking has remained the same since its invention in the 1930s [1]. However, design and implementation of PLLs continue to be challenging as design requirements of a PLL such as clock timing uncertainty, power consumption and area become more stringent.

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL tracks the phase changes that are within the bandwidth of the PLL.

A PLL is a negative feedback control system circuit. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals. The overall goal of the PLL is to match the reference and feedback signals in phase, this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

A basic form of a PLL consists of five main blocks:

1. Phase Frequency Detector (PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Frequency divider

3. PLL Architecture

To synchronize the frequency, various types of PLLs are being used in the application of wireless communication. PLLs are consists of PFD, CP, LPF, CSVCO and divider which is shown in Fig. 1. In addition with CSVCO, the PFD compares feedback signal

with input signal and generates the error signal. A charge pump circuit along with LPF is used to minimize the disturbances at the input of CSVCO and to get a sharper and smooth signal at the CSVCO output. To form a phase-locked loop (PLL), the phase error output of PFD is fed to a charge pump and then to loop filter which integrates the signal to get a sharper and smooth signal so that the disturbances at the input of CSVCO get minimized.

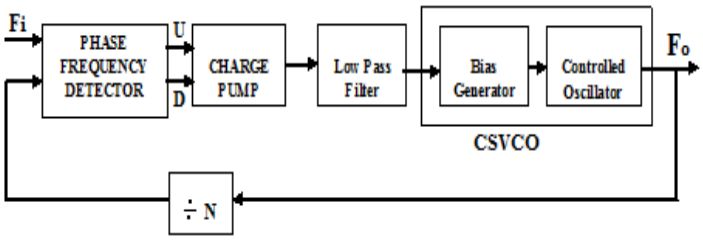

Fig. 1: Architecture of PLL.

4. Current-starved Voltage Controlled Oscillator

The operation of current starved VCO is similar to the ring oscillator. Fig. (2) shows a one stage Current Starved VCO [6]. Middle PMOSM1 and NMOSM2 operate as inverter, while upper PMOSM11 and lower NMOSM14 operate as current sources. The current sources limit the current available to the inverter. In other words, the inverter is starved for current. The current in the first NMOS and PMOS are mirrored in each inverter/current source stage. PMOSM11 and NMOSM11 drain currents are the same and are set by the input control voltage [6].

The current-starved VCO is as shown in Fig. (2) With the current-starved structure, the supply noise would contaminate the output phase. Referring to (6), the output frequency can be assumed to be in terms of the RC delay and n denoting the number of the inverter stages. C_{tot} denotes the total parasitic capacitance including wire parasitic capacitor (C_{wire}), and drain-to-bulk capacitor (C_{DB}). Moreover, the resistance of the channel of each stage (R) could be estimated as the reciprocal of the transconductance of the MOS With $\emptyset_0 = \frac{df_0}{dt}$ the supply noise would change the V_{GS} of the PMOS and further affect the output frequency and output phase, where V_{TH} denotes the threshold voltage [11].

$$f_0 \, \alpha \, \frac{1}{n.R.C_{tot}}$$

$$f_0 = \frac{g_m}{n.C_{tot}} = \frac{\mu \, C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})}{n.C_{tot}}$$

This VCO is designed using ring oscillator and its operation is also similar to that. From the schematic circuit shown in the Fig. (3), it is observed that MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for the current. The MOSFETs M5 and M6 drain currents are the same and are set by input control voltage, which is varied in the

steps of 0.5V, starting with 5V. The currents in M5 and M6 are mirrored in each inverter/current source stage. There are in total 23 transistors, where upper PMOS transistors are connected to the gate of M6 and source voltage is applied to the gates of all lower NMOS transistors [9].

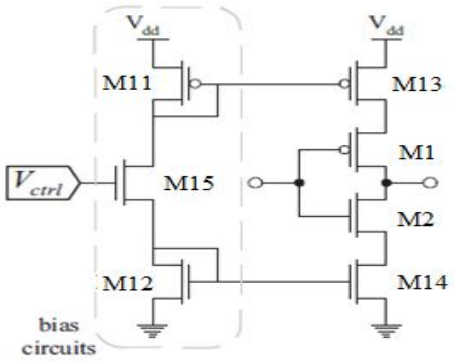

Fig. 2: Current starved with output-switching.

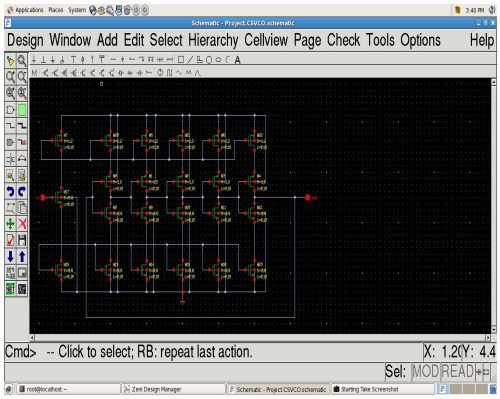

Fig. 3: Schematic Circuit of Current-Starved VCO

5. Phase Frequency Detector

A phase frequency detector (PFD), is a device which compares the phase of two input signals and provides a signal in the form of phase error. It has two inputs which correspond to two different input signals, usually one from a current starved voltage-controlled oscillator and other is a reference source. It has two outputs which instruct subsequent circuitry on how to adjust to lock onto the phase [10].

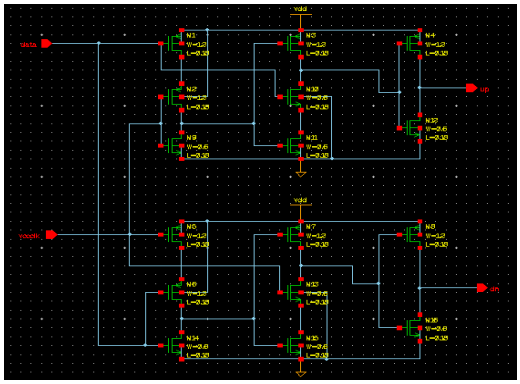

Fig. 4: Schematic Circuit of Phase Frequency Detector.

From Fig. (4) the Schematic Circuit of Phase Frequency Detector compares the leading edges of data and data1 (data is the input signal to PFD, data1 is considered as the feedback signal from the output of VCO to PFD). A data1 rising edge cannot be

present without a data rising edge. If the rising edge of the data leads the data1 rising edge, the "Up" output of the phase detector goes high while the "Down" output remains low. This causes the data1 frequency to increase and makes the edges move closer. If the data1 signal leads the data, "Up" remains low while the "Down" goes high. And we can find the phase difference between data1 and data.

6. Charge Pump

A charge pump circuit is used to convert the digital signal from the phase frequency detector to analog signal, the output of which is used to control the frequency of the voltage control oscillator. The output of the PFD should be combined into a single output to drive the loop filter. In Fig. (5) charge pump, two NMOS and two PMOS are connected serially. The uppermost PMOS and lowermost NMOS are considered as the current source and the other PMOS and NMOS in the middle are connected to the "Up" and "Down" of the output of PFD, respectively When the PFD "Up" signal goes high, the PMOS will turn on. This will connect the current source to the loop filter. It is in the similar way when the PFD "Down" signal goes high.

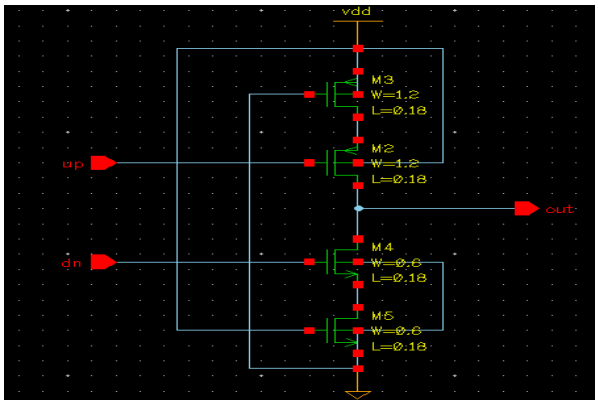

Fig. 5: Schematic Circuit of Charge Pump.

7. Loop Filter

Filters are frequently added after the charge pump to reduce the ripple. The function of the loop filter is to convert the output signal of phase frequency detector to control voltage and also to filter out any high frequency noise introduced by the PFD. The loop filter shown in Fig. (6) used with this type of PFD is a simple RC low-pass filter. Since the output of the PFD is oscillating, the output of the loop filter will show a ripple as well, even when the loop is locked. This modulates the clock frequency, an unwanted characteristic of a DPLL using PFD. A ripple on the output of the loop filter with a frequency equal to the clock frequency will modulate the control voltage of the VCO. A high speed low power consumption positive edge triggered Delayed (D) flip-flop was designed for increasing the speed of counter in Phase locked loop, using 180 nm CMOS technology.

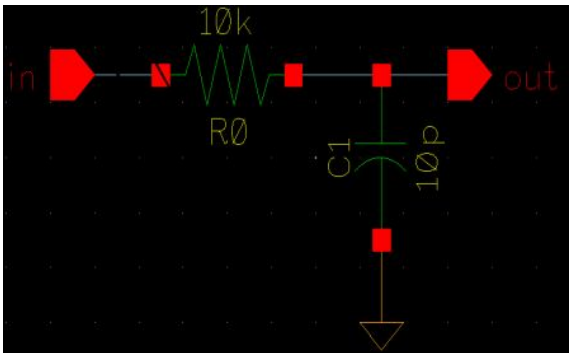

Fig. 6: Low Pass Filter.

8. Frequency Divider

Frequency divider divides the VCO frequency to generate a frequency which is comparable with reference frequency. Here we used divide by 2 network, we can vary the divider network for synthesis of different frequencies. It divide the clock signal of VCO and generate dclock as shown in Fig. (7), than applied to phase frequency detector which compare it with input data[8].

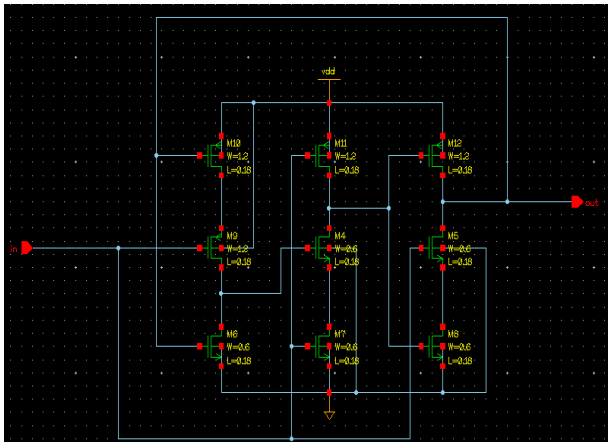

Fig. 7: Schematic Circuit of Frequency divider.

9. Results and Waveforms

The PLL for high performance application have been designed using 180 nm CMOS technology with 36.516 mA. and emulated by Zeni Electronic Design Automation . The phase noise obtained is-122.2 dBc/Hz @ 10 MHz offset frequency, which is shown in Fig. (8). The proposed voltage controlled oscillator has designed for getting optimized 2.2 GHz frequency. A design has been completed with 180 nm CMOS technology and 1.5 Volt supply voltage. The final output waveform of complete PLL is shown in Fig. (9). Where signal1 is for input data signal coming to phase frequency detector, signal2 is for output of PFD UP signal, signal3 is for output of PFD DN

signal, signal4 is output charge pump, signal5 is output of Low Pass Filter, signal6 is output of current starved voltage controlled oscillator, and signal7 is output of divider circuit that is performing divide by 2 operation which is second input to the phase frequency detector.

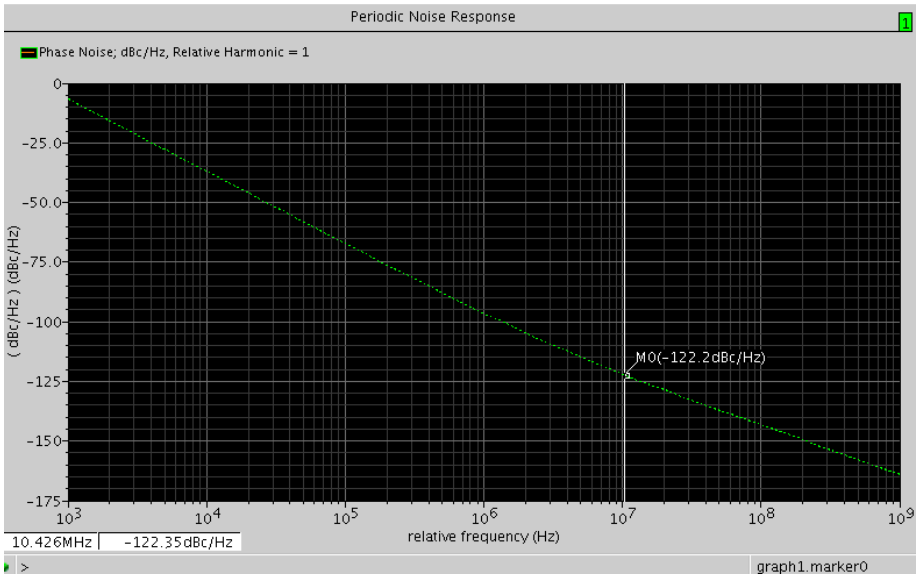

Fig. 8: Phase noise response of CSVCO @10 MHz offset frequency.

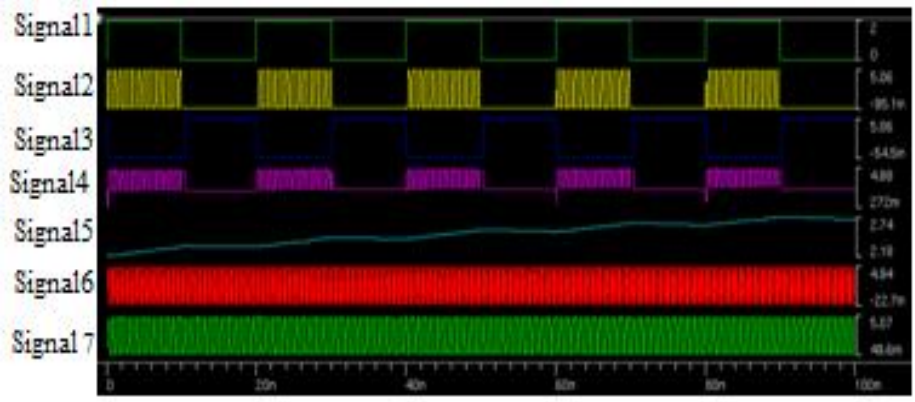

Fig. 9: waveforms of different stages of output signal for PLL.

10. Conclusion

Modern wireless communication system employ phase locked loop (PLL) mainly on synchronization clock synthesis, skew and jitter reduction. Because in the increase of speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. The PLL has been designed with low power, small chip size area and better phase noise using 180 nm CMOS technology for high performance PLL and simulated

by ZENI EDA environment. While increasing the number of stages for getting the higher frequency the power dissipation and size of oscillator was going to increase. Hence instead of increasing the number of stages and time constant again a control voltage and width of the CMOS can be adjusted for getting the higher frequency.

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