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Scaling – Its Effect on Leakage Reduction

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Abstract

This document presents the effects of scaling towards leakage power reduction. Scaling advanced CMOS technology to the next generation improves performance, increases transistor density, and reduces power consumption. Recent research has revealed that with the gradual shrinking of device sizes, the leakage power dissipation is becoming more and more dominant, and it is likely to become comparable to switching power dissipation in future generation VLSI circuits. This has motivated us to develop suitable technique for the reduction of leakage power dissipation in CMOS circuits. In this paper, a conventional CMOS inverter is scaled to different PMOS channel widths and it is implemented with a leakage reduction technique, Stacking. The results are simulated on a SPECTRE simulator of the Cadence virtuoso tool. At constant channel length, by applying this technique, the reduction of leakage power and optimal performance of the circuit can be observed. With the change in channel width of PMOS transistor, there is change in the number of charge carriers flowing through the channel which shows the reduction in current that leads to reduction in leakage power.

Keywords: CMOS; Scaling; Leakage power; Stacking; PMOS width; Spectre.

1. Introduction

In the past, the major concerns of the VLSI designers were performance and miniaturization. With higher speed and density of CMOS circuits, power dissipation has become a growing concern [1]. Leakage currents, are mainly responsible for static power dissipation during idle mode, they are increasing dramatically in sub-100nm

processes. Sub threshold leakage rises due to threshold voltage scaling while gate leakage current increases due to scaling of oxide thickness. Different types of leakage mechanism and their reduction techniques [2] are available and in this paper transistor stacking with the concept of scaling applied to it has been analyzed keeping supply voltage, process technology constant [7]. If this trend continues, leakage power will soon be comparable to dynamic power. Estimating leakage power in early stages of VLSI circuit design is important for optimizing the total power dissipation [3].

1.1 Scaling

In early 1970's it was noted that the MOS transistor has a new and unique property that the basic transistor structure could be comprehensively reduced to a smaller dimension and this is called scaling. Scaling factor λ, is the fractional size reduction from one generation to the next [4].

$$L_{min} \rightarrow \lambda \cdot L_{min}, \quad t_{ox} \rightarrow \lambda \cdot t_{ox}, \quad V_{dd} \rightarrow \lambda \cdot V_{dd}$$
$$V_t \rightarrow \lambda \cdot V_t, \quad NA \rightarrow NA/\lambda, \quad x_j \rightarrow \lambda \cdot x_j$$

1.2 Stacking

Sub-threshold leakage current flowing through a stack of series-connected transistors reduces when more than one transistor in the stack is turned off. This effect is known as the stacking effect [2]. Due to the stacking effect, the sub-threshold leakage through a logic gate depends on the applied input vector. For a circuit with n primary inputs, there are 2^n combinations for input states [5]. This method involves generating a large number of primary inputs, evaluating the leakage of each input, and keeping track of the best vector giving the minimal leakage current [6].

2. Proposed Design

Fig. 1 (a) depicts the CMOS Inverter with PMOS width set to 'w', on which the parameter 'w' is swept in a certain range of values and simulated to find power dissipation. Hence with the scaling in width (w), change in power dissipation is being analysed.

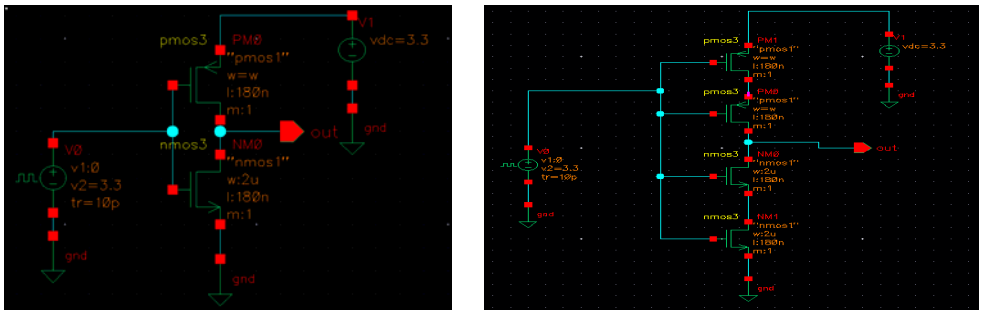

Figure 1: (a) Conventional CMOS Inverter, (b) CMOS Inverter with transistor stacking.

Fig. 1 (b) depicts the CMOS Inverter with transistor stacking with PMOS width set to w, on which parametric sweep is simulated to enumerate reduction in power dissipation. Here, NMOS width is set to 2 um and PMOS width is set to 'w' whose parametric sweep is to be done, while channel length is at 180 nm. In transistor stacking [8], series connected stack transistors are used and there is reduction in the transistor widths to half as that of the conventional CMOS Inverter. The above circuit produces the output same as that of the conventional CMOS Inverter, but there is reduction of leakage power dissipation; hence, the total power dissipation also reduces [9].

3. Design Equations

To determine the design equations for use with calculation of leakage power, the leakage current has to be estimated using equation:

$$I_{leak} = u_0 C_{ox} W/L (m-1) (V_T)^2 \exp (V_g-V_{th})/mV_T (1-\exp-(V_{DS}/V_T)) \quad (1)$$

Where,

$$m = 1 + C_{DM}/C_{OX} = 1 + 3t_{ox}/W_{DM} \quad (2)$$

The leakage power can be calculated using equation shown below in which I_{leak} can be calculated using equation (1).

$$P_{leak} = I_{leak} * V_{DD} \quad (3)$$

The leakage power calculated above can be reduced using stacking technique and effect of the scaling on stacking is shown below in simulation results [10].

4. Simulation Results

In this paper, the power dissipation of conventional CMOS Inverter with transistor stacking has been compared. The results are simulated on Cadence Virtuoso tool having SPECTRE simulator. The total power dissipation of CMOS Inverter is calculated as 75.102uw, while that of CMOS Inverter with stacking is 41.156 uw, while leakage power is reduced to about 0.243 pw from 3.423 pw. This shows the reduction of leakage power using stacking technique, which tends to the reduction of total power dissipation.

Fig. 2 depicts the dc characteristics of CMOS Inverter with applied stacking technique with different PMOS widths for leakage power reduction. Above figure shows the variation of output voltage considerable from nearly 0.7 V. to 2.7 V., in this range more leakage current flows, since in this region, the switching of the PMOS and NMOS happens, hence here dynamic leakage current will flow.

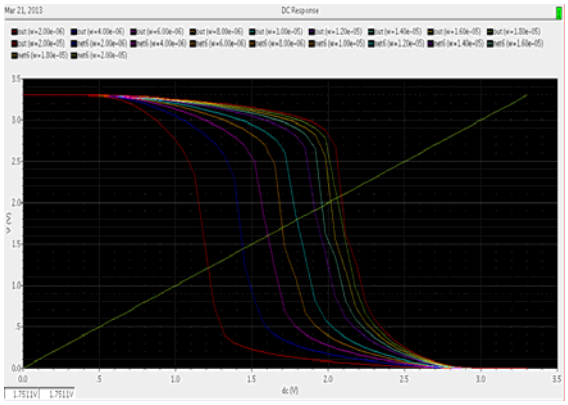

Figure 2: DC Characteristics of CMOS Inverter with Stacking at different PMOS widths.

Fig 3 (a) below shows the leakage current of the fig. 1 (b). It shows the variation of leakage current with different widths, it is due to the variation of channel carriers at different channel width which tends to variation of leakage power and the total output power.

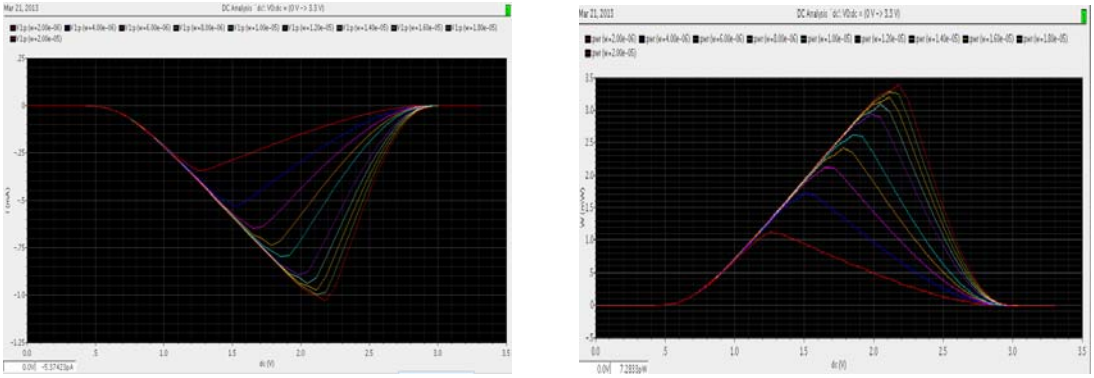

Figure 3: (a) Leakage current v/s Input voltage characteristic, (b) Output power of CMOS Inverter with Stacking.

From the results of leakage current, leakage power can be calculated using equation (3), the simulated result below shows the total power waveform of CMOS Inverter with stacking. Fig. 4 below depicts the power v/s width graph of CMOS Inverter with transistor stacking. This graph is drawn at various PMOS width at different input voltages.

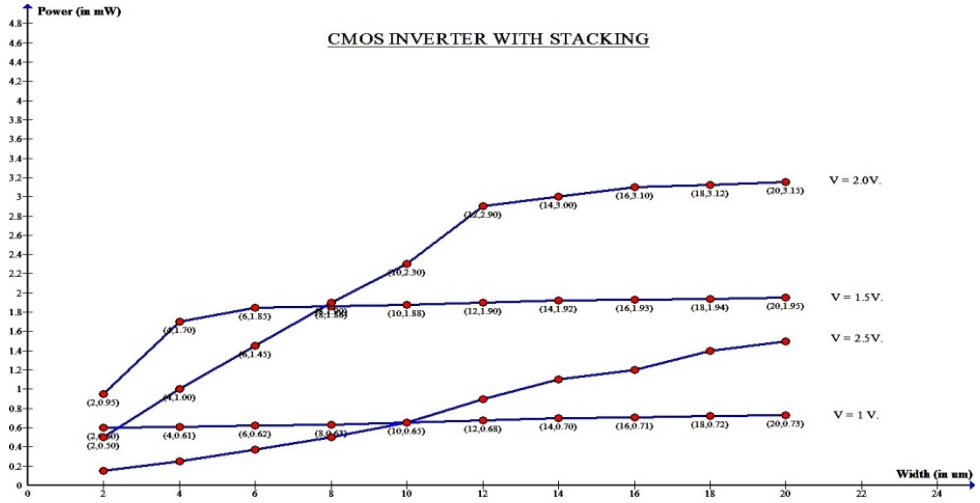

Figure 4: Power v/s Width Graph.

Below table shows the comparison between the power of conventional CMOS Inverter and CMOS inverter with stacking at different PMOS width's.

Table I: Power and Width at different supply voltages.

Width (um.)	Conventional CMOS Inverter Power (mW.) at				CMOS Inverter with Stacking Power (mW.) at			
	V = 1V.	V = 1.5V.	V = 2V.	V = 2.5V.	V = 1V.	V = 1.5V.	V = 2V.	V = 2.5V.
2	1.40	1.93	1.10	0.35	0.60	0.95	0.50	0.15
4	1.41	2.95	2.10	0.60	0.61	1.70	1.00	0.25
6	1.42	3.10	3.00	0.90	0.62	1.85	1.45	0.37
8	1.43	3.14	3.95	1.20	0.63	1.86	1.90	0.50
10	1.44	3.18	4.40	1.60	0.65	1.88	2.30	0.65
12	1.45	1.20	4.70	2.20	0.68	1.90	2.90	0.90
14	1.47	3.24	4.78	2.60	0.70	1.92	3.00	1.10
16	1.48	3.26	4.80	3.00	0.71	1.93	3.10	1.20
18	1.49	3.28	4.85	3.30	0.72	1.94	3.12	1.40
20	1.50	3.30	4.90	3.60	0.73	1.95	3.15	1.50

5. Conclusions

A new design of CMOS Inverter with stacking is proposed which uses the concept of scaling the channel width of PMOS. Based on results of our simulation, we suggest varying the PMOS width in a certain range where leakage reduction can be observed.

We observe that using the proposed circuit, there is reduction of about 45% in the power consumed with respect to the conventional circuit with different PMOS widths. More leakage reduction can be observed by using dual threshold technique of leakage power reduction in place of stacking technique.

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