Advance in Electronic and Electric Engineering.
ISSN 2231-1297, Volume 3, Number 8 (2013), pp. 951-958

http://www.ripublication.com/aeee.htm

A New CMOS Low Drop-Out Regulator with Improved PSRR

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Abstract

Low-dropout regulators (LDO) are widely used in electronics products due to their precision output voltage and less prone to noise. The advancement in battery operated portable devices, noise sensitive devices and other devices, which need high precision supply voltages has fuelled the growth of Low Drop-Out Regulators. Low Drop-Out Regulators have shown advantage over its counterpart. The design of Low Drop-Out Regulators with high performance is challenging problem now-a-days. The increasing demand, however, is especially apparent in mobile battery operated products, such as cellular phones, pagers, camera recorders, laptops etc.

In this paper, A CMOS Low Drop-out Regulator with improved PSRR is proposed. The proposed circuit is developed using error amplifier, subtractor circuit and PMOS as pass device. For the improvement of dc PSRR, a subtractor circuit is introduced along with two stage error amplifier with NMOS mirror load in conventional low drop-out regulator topology. The proposed circuit is simulated using TSMC 0.18μm CMOS technology process parameters. The proposed LDO has regulation range of 1.25-1.8V and for this range output voltage is 1.2V.The proposed LDO has high dc PSRR of -57.68 dB and PSRR bandwidth of 95 KHz. The performance parameters of the proposed LDO has also been compared with the existing LDO circuits available in literature and the comparison shows that the proposed LDO has wider bandwidth range of PSRR with better dc PSRR.

Keywords: CMOS; Compensation; LDO; PSRR.

1. Introduction

Conditioning and supplying of power are the most elementary functions of an electrical system. Any loading application, be it a cellular phone, pager, or wireless sensor node, cannot sustain itself without energy, and cannot fully perform its functions without a stable supply. The fact is transformers, generators, batteries, and other off-line supplies incur substantial voltage and current variations across time and over a wide range of operating conditions. They are normally noisy and jittery not only because of their inherent nature but also because high-power switching circuits like central-processing units (CPUs) and digital signal-processing (DSP) circuits usually load it. These rapidly changing loads cause transient excursions in the supposedly noise-free supply, the end results of which are undesired voltage drops and frequency spurs where only a dc component should exist [1]. Use of switching power supply or DC to DC converter, provides portable applications, which makes those systems to operate in noisy environments. Mostly electronics systems are very sensitive to noise present on power supply. Consequently, they need large battery filters to reduce the ripple on battery voltage [2]. The explosive proliferation of battery-powered equipment in the past decade has accelerated the development and use of Low-Dropout voltage regulators for noise sensitive circuits [2, 3]. Low drop-out regulators is driven by the growing demand for higher performance power supply circuits [4]. The low drop-out nature of the regulator makes it appropriate for use in many applications, namely, automotive, portable and biomedical applications. The increasing demand, however, is especially apparent in mobile battery operated products, such as cellular phones, pagers, camera recorders, and laptops. In a cellular phone, for instance, switching regulators are used to boost up the voltage but LDO's are cascaded in series to suppress the inherent noise associated with switchers. LDO's benefit from working with low input voltages because power consumption is minimized accordingly, $P= I_{Load} * V_{in}$. Low voltage and low quiescent current are intrinsic circuit characteristics for increased battery efficiency and longevity. Low voltage operation is also a consequence of process technology. This is because isolation barriers decrease as the component densities per unit area increase, thereby exhibiting lower breakdown voltages. Therefore, low power and finer lithography require regulators to operate at low voltages, produce precise output voltages, and have characteristically lower quiescent current flow [5]. The thrust is towards reducing the number of battery cells, required to decrease cost and size, while maintaining power supply rejections and other specification of regulators [6].

2. Low Drop-Out Regulator with Improved PSRR

Low drop-out regulators are essential analog building blocks that shield a system from fluctuation in supply rails. The importance of determining their power supply rejection ratio performance is magnified in SoC systems. Power supply rejection ratio (PSRR) is ripple rejection ability of the circuit to reject the ripple of power supply at various frequencies.

The proposed low drop-out regulator is designed to improve power supply rejection ratio (PSRR) of the conventional LDO. In conventional LDO topology, the output of error amplifier is proportional to the gate capacitance of pass device that provides a better PSRR value. To further improve the PSRR value, one block (B1) [7] is used in the conventional LDO topology [6] as shown in Figure 1.

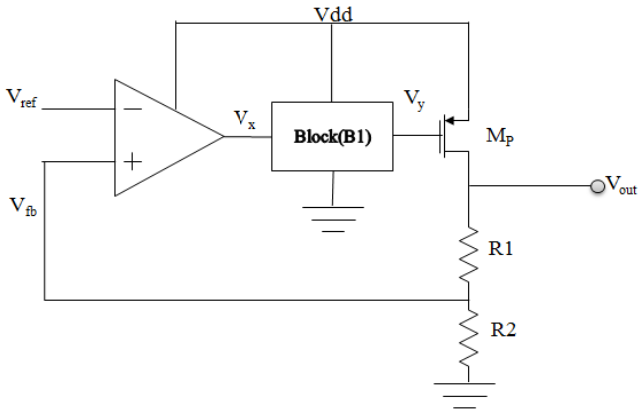

Figure 1: Proposed low drop-out regulator block diagram.

The circuit diagram of proposed CMOS low drop-out voltage regulator with improved PSRR is shown in Figure 2. The output of error amplifier (V_x) is proportional to the gate capacitance of pass transistor so it will provide better PSRR. The transistors (M1-M8) are used to form the error amplifier, transistors (M9-M10) are used to form the block (B1), M_P is the pass transistor, and passive elements R1 and R2 are used to form the feedback network to provide feedback voltage (V_{fb}) to the error amplifier.

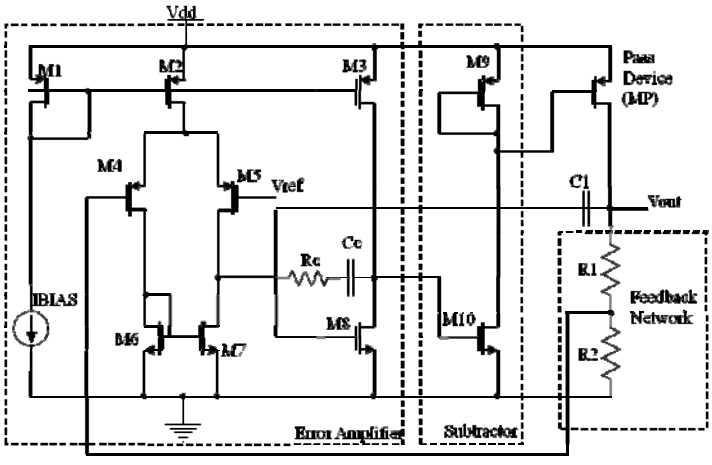

Figure 2: Circuit diagram of proposed low drop-out regulator.

The compensation capacitor C_1 connected between output terminal and gate of transistor M8 is used to reflect the miller capacitance as the gain of three stages for better stability. The RC compensation formed by R_C and C_C, is used to improve the stability of two stage error amplifier.

3. Simulation Results

The proposed low drop-out regulator circuit has been simulated using TSMC 0.18µm CMOS technology process parameters. Figure 3 (a) and (b) show the frequency responses of proposed CMOS Low drop-out regulator with improved PSRR.

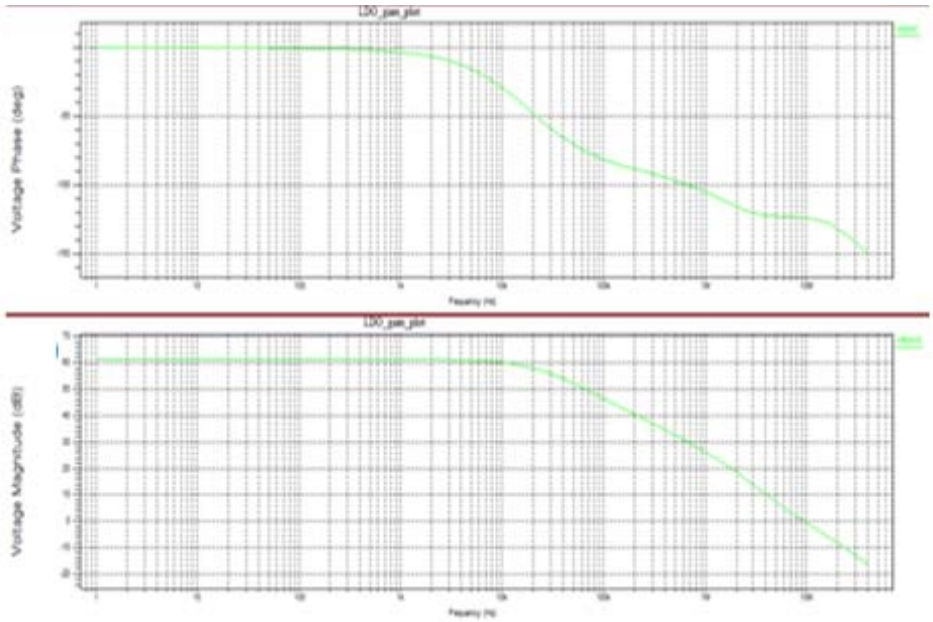

Figure 3: Frequency response of proposed LDO (a) Phase vs. Frequency (b) Gain vs. Frequency.

From Figure 3, it is observed that proposed LDO has gain of 62 dB and phase margin of 61 degree. Hence, the proposed LDO is stable as it shows phase margin of 61 degree, which is more than required 60 degree phase margin. The plot of output voltage (V_{out}) vs. input voltage (V_{dd}) is shown in Figure 4. From Figure 4, it is observed that the regulation range of proposed LDO is 1.25 to 1.8V and for this range the output voltage is 1.2V.

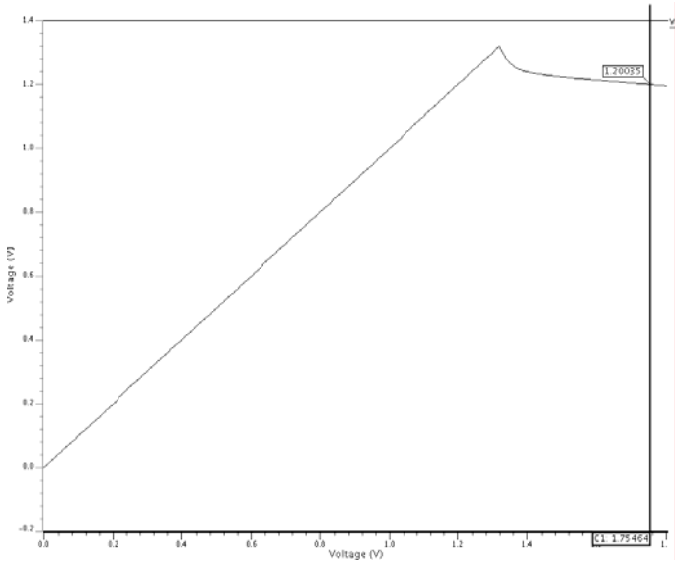

Figure 4: Plot of output voltage versus input voltage.

The Plot of PSRR of proposed LDO is shown in Figure 5. From Figure 5, it is observed that the proposed LDO has high dc PSRR of -57.68 dB and PSRR bandwidth of 95 KHz. It is also observed that by the use of block (B1), better dc PSRR with wider PSRR bandwidth has been achieved.

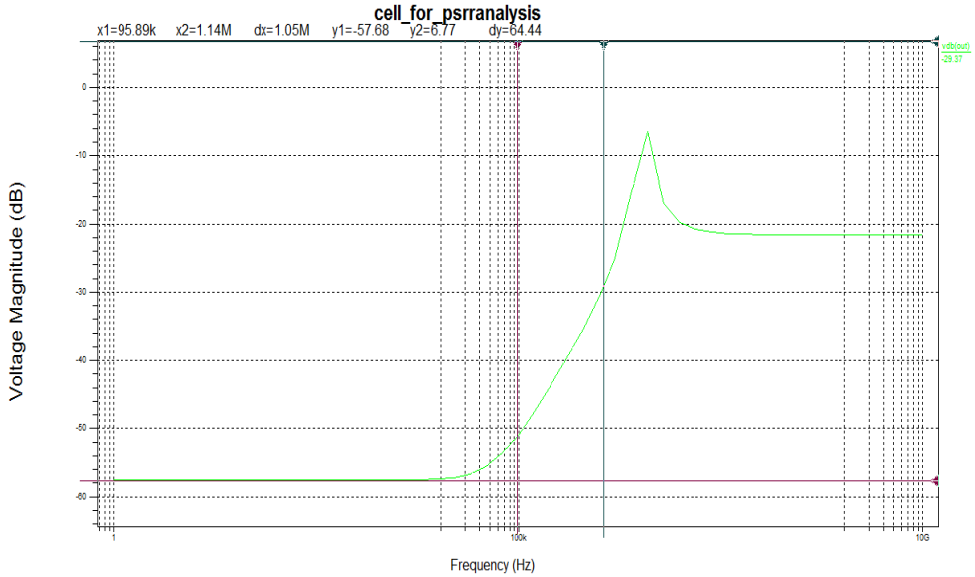

Figure 5: Plot of PSRR of proposed LDO.

Table 1 compares the performance parameters of proposed CMOS low drop-out regulator with improved PSRR with the existing low drop-out regulators available in literature. From the table, it is observed that the proposed circuit has wider range of PSRR with better dc PSRR.

Table 1: Comparison of proposed circuit with the LDOs available in literature [8-16]

Circuit Parameters	[10]	[8]	[9]	[12]	[15]	[16]	[14]	[11]	[13]	Proposed LDO
Year	2004	2006	2007	2008	2009	2009	2010	2012	2012	2013
Technology (µm)	0.5	0.5	0.35	0.35	0.35	0.18	0.18	0.18	0.18	0.18
Input voltage range (V)	3.3	2.8-3.8	2.5-5.5	1.2	3-5	1.2-1.8	4.0-5.5	2.0-3.2	3.0-5.0	1.25-1.8
Output Voltage (V)	2.8	1.8	1.8	1.0	2.5	1.0	2.8	1.25	2.8	1.2
PSRR (dB)	-	-30dB at 20KHz	45dB at dc	-30dB at dc	-75dB at 1kHz	-41dB at 1KHz	-69dB at dc	64.3dB at dc	-56dB at dc	-57.68dB at dc, -31dB at 1MHz
PSRR BW (KHz)	-	-	20KHz	-	1kHz	1KHz	25KHz	<1KHz	-	96 KHz
Gain (dB)	55dB	58dB	61dB	-	-	-	-	40dB	60dB	62dB
Phase Margin (Degree)	60°	60°	65°	-	-	-	-	-	63°	61°
Load Capacitor CL (µF)	2.2 µF	2.2 µF	1 µF	-	3 µF	-	-	(0.47-4.7) µF	1 µF	-
Load Current IL (mA)	23	20	-	-	-	50 mA	25 mA	-	-	40mA

4. Conclusion

Low Drop-Out Regulators are capable of keeping their specified output voltage over a wide range of load currents and input voltages. Low Drop-Out Regulators provide constant supply rail for integrated circuits. Many of the Low Drop-Out Regulators in today's portable devices are integrated into multifunction Power-management integrated circuits. Stability is major concern for Low Drop-Out Regulator design, which can be achieved by either using external capacitor or by using some special compensation techniques. Low Drop-Out Regulator has found applications in portable devices for power management. In this work, a CMOS low drop-out regulator with improved PSRR has been developed. The proposed circuit provides an output voltage of 1.2V for the input voltage range of 1.25 to 1.8V. The proposed circuit has been compared with the existing circuits available in the literature and it has been observed that the proposed circuit has better PSRR bandwidth while maintaing the dc PSRR at appropriate level.

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