

Effect of Sunlight Radiation on Data Stored in Double Data Rate Synchronous Dynamic Random Access Memory in Katsina and Kaduna States, Nigeria

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Abstract

This research focuses on investigating the effect of exposing two types of double data rate SDRAM memories to solar radiation in order to see whether this can caused data loss in them. Three DDRI and three DDRII memory samples were randomly selected and connected to dual DIMM slots of desktop computer, from where they were tested for data loss using diagnostic software version V1.45a, before and during their exposed to sunlight. The tests were carried out, by loading and running diagnostic software version V1.45a from CD-ROM drive of a desktop computer. Six data collection centers, three in Kaduna state and three in Katsina state, Nigeria were selected to cover the minimum, medium and maximum solar insolation of the case study area. An experimental setup was used consist of computer system loaded with above software from a CD and DDRI and DDRII samples were connected to dual DIMM slots of the computer. The poynting vector of solar radiation incidented the samples, the atmospheric temperature and relative humidity of the environment under which the experiments for data collection were conducted were measured using solar data logging meter and MOSTEC multimeter and this form part of the experimental setup. Results obtained show that, for the six samples tested before irradiation they have residual fault in them which are not due to their exposure to sunlight. The percentages of the faults obtained are 6.3%, 25.4%, 12.5% and 6.25% faulty memory address locations, depending on their data storage capacities of the samples tested. The same % of faulty memory address locations were recorded, during exposure to sunlight and testing of the six samples with sunlight. In continuation of

the test, after two DDRII were irradiated with sunlight and tested for twelve hours, they had developed hardware faults in them. Fault models were detected by the diagnostic software in the six memories namely: address bit error, stuck at fault, short between adjacent columns and data lines, burst functionality failure during read or write cycle. This work concludes that through irradiation of two in number DDRII with sunlight for twelve hours each at an average certain average temperature and relative humidity, this can develop hardware fault in them.

Keywords: Sunlight radiation, Synchronous dynamic, Random access memory, Kaduna and Katsina States.

1. Introduction

Microcontrollers systems, ATM machines, servers, networked or un-networked computers are globally used for different applications like control, data processing, sharing and exchanging of information on LAN, internet. This has tremendous contributed towards the growth of national economies. These technologies are presently applied in almost all economic sectors of countries like Nigeria, such as energy, health, education, banking, insurance, manufacturing and electric power utilities. One of the main building blocks of these technologies are semiconductor memories which function as their temporary data storage devices. Data loss or soft error in the data storage devices of these technologies would affect their functions and consequently it would affect the economy of countries, organizations and individuals. Saha, 1995 stated that data loss in internal memories can be caused by environmental factor like radiation particles striking memory chip. Soft errors occur because of the unintended transitions of logic state in a circuit, typically caused by external source of ionization radiations that creates excess free carriers, which recombine with the store charges, thereby corrupting the state of transistor (Garg, n.d). The functions and reliabilities of above technologies can be affected due to carelessness of man like their exposure to powerful electromagnetic radiation sources, such as sunlight, EM radiation from mobile phone based transceiver substations(BTSs) installed and operated in residential, industrial, commercial and administrative areas. Paul (2009) stated that, "the five reasons of data loss in computers are: hardware failure; firmware corruption; malicious work of people who develop viruses; human error; and computer operating system failure". Data loss or error in synchronous dynamic random access memory (SDRAM) based systems like computers have been a concern for longer period of time, and can be explained as an event that leads to the logical state of one or multiple bits of semiconductor memory being read differently from how they were written. Schroeder, Pinheiro, and Weber (2011) stated that, "memory errors can be caused by electrical or magnetic interference, and this can be due to problems with hardware (example, a bit being permanently damaged), or it can

be as a result of corruption along the data path between the memories and the processing elements. They are of the opinion that DRAM error behaviour in the field differs in many key aspects from commonly held assumptions. Also Schroeder, Pinheiro, and Weber, (2011) reported that DRAM error rates due to ionization radiation such as gamma ray, are of the order of magnitude higher than previously reported, with 25,000 to 70,000 errors per 10^9 device hours per Mb, and more than 8% of DIMMs affected by errors per year.

This study arises due to failure of dynamic random access memory (DRAM) found in semiconductor memory based systems, when exposed to ionization radiations, like the constant exposure of computer system to sunlight radiation due to human negligence. In this study a desktop computer containing DDRI and DDRII connected to its DIMM slots will be exposed to sunlight radiation, and a memory diagnostic software will be run from the same computer, to test the DDRI and DDRII for software error or hardware error due to this exposure.

2. Electricity Conduction in Semiconductors Due to Photons Absorption

Due to the above exposure, the valence electrons of the semiconductor would absorb sunlight photons, when its energy is equal or greater than its work function (forbidden energy gap) of the material, therefore transitions of electrons occur from the valence band maximum to the bottom of the conduction band minimum, leaving equal number of holes in the valence band. Qing, (2002) stated that "If the conduction band minimum and the valence band maximum is at the same position in K-space, it is called a direct band gap. The band structure of doped semiconductor is shown in Figure 1. Setting the wave vector k equal to 0, the donors and acceptors formed levels in the energy gap region. At temperature equal to 0 K, any free carriers from donors and acceptors are bound to their atoms. So there is no conduction. At room temperatures, the sites can be thermally ionized, releasing carriers in the bands, so conduction can occur.

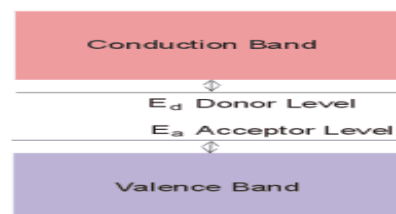


Figure 1: Band structure of doped semiconductor material.

The valence band maximum is at k equal to 0, is known as the gamma point. Where the conduction-band minimum also occurs at k equal to 0, the semiconductor is

said to be a direct band semiconductor. At non zero temperature and k equal to 0, the semiconductor can be an indirect band semiconductor. In III-V semiconductors, that is Ge and Si, there are three valence bands with maxima at k equal to 0. These are the light hole, heavy-hole and spin-orbit split-off band. If electro-electron interaction is disregarded, and the Coulomb interaction between electrons and holes are treated as small perturbations, the calculated energy of a electron and a hole from the quantum perturbation theory is (Qing, 2002):

$$E_l(k) = E_g - \frac{1}{2m_e^*} + \frac{1}{2m_h^*} \dots \quad (1)$$

Where,

$$\frac{1}{m_e^*} = \frac{1}{m_0} + \frac{1}{m_1} + \dots \quad (2)$$

,here the effective mass of electron and the hole, E_g the band gap and integer the quantum number of the excitant. And a rough approximation of ionization temperature is:

$$\dots \quad (3)$$

The numbers of ionized donor and acceptor sites are:

$$\dots \quad (4)$$

$$\dots \quad (5)$$

2.1 Silicon Semiconductor Band Structure Model

Semiconductor band structures in general and especially for silicon as shown in Figure 2. The plot is drawn for energy values along particular edges of the irreducible wedge, cf. Figure 2(b). For silicon the conduction band minima lie on the six equivalent $\langle 100 \rangle$ -directions and occur at about 0.85% of the way to the zone boundary, see Figure 2(b).

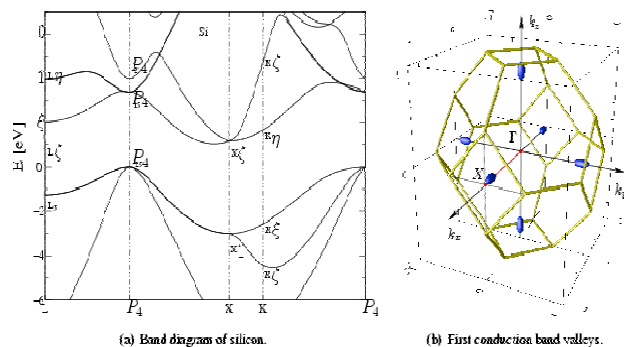


Figure 2a and 2b: Silicon band energy diagrams.

These are the well-known, equivalent ellipsoidal constant energy valleys. When electrons gain 0.13eV of energy, they can cross the zone boundary. Wessner, (2006) stated that "The simplest model of the silicon band structure is based on the effective mass. If the band structure is known, the energy wave vector relation in one dimension can be expanded in a Taylor series as"

$$E(\kappa) = E(0) + \frac{\partial E(\kappa)}{\partial \kappa} \bigg|_{\kappa=0} \kappa + \frac{1}{2} \frac{\partial^2 E(\kappa)}{\partial^2 \kappa} \bigg|_{\kappa=0} \kappa^2 + \dots \dots (6)$$

Band structures of materials like Si GaAs, SiO₂ and diamond are well described by Tight Binding Hamiltonians on the basis of atomic sp³ orbitals.

2.2 Propagation of Electromagnetic Radiation in Semiconductor

Double data rate synchronous dynamic random access memories are made up of MOSFET electronic switches and MOS capacitors (lossy dielectrics). The propagation of EM in them is characterized by the following EM radiation vector equations in exponential form (Kumari and Subasri 2007):

$$E(z, t) = E_0 e^{-\alpha z} \cos(\omega t - \beta z) a_x \dots (7)$$

$$H = (E_0 / \eta) e^{-\alpha z} \cos(\omega t - \beta z - \theta_\eta) a_y \dots (8)$$

Where α is the attenuation coefficient of the medium (semiconductor) and β is a measure of phase shift per unit length. At any time, E leads H by θ as the wave propagates in the medium. According to Kumari and Subasri 2007, the average value of the poynting vector of the incoming wave at the air-semiconductor boundary, falling perpendicular on the plane of the semiconductor memory module over a given period of time is given by:

$$P_{av} = \frac{E_0 \times H_0}{2} \dots (9)$$

Poynting 's theorem can be applied to the total EM power density propagated into the memory module and the rate of decrease of its electric and magnetic components of the wave in the medium and the ohmic power dissipated in it, is given by (Kumari and Subasri 2007):

$$\oint_s (E \times H) \cdot ds = -\partial/\partial t \int_v (\frac{1}{2} \epsilon E^2 + \frac{1}{2} \mu H^2) dv - \int \sigma E^2 dv \dots (10)$$

The plastic package of DDR SDRAM is made up of Bismaleimide Triazine (BT). The value of its dielectric constant for electrostatic fields is 4.2. The values of dielectric constants are inversely proportional to angular frequency of the applied fields. At sunlight frequencies of 4×10^{12} Hz to 8×10^{15} Hz, the BT dielectric constant reduced drastically, due to dielectric dispersion, which caused the induced polar polarization in

the BT to lose changes due to oscillation of applied electric field component of sunlight. BT is not a magnetic material, therefore the value of the magnetic field component of sunlight poynting vector propagated in it approaches zero. It is the ohmic resistant of the BT which caused heat dissipated as the wave propagate in it, in the form of heat, and the electric component of the wave decreased as it propagated and caused distortion polarization in it.

2.3 Theory on Data Loss in Semiconductor Memories Due to Solar Radiation Absorption

At room temperature and under light illumination, nearly all the impurity/defects sites in the semiconductor are thermally ionized (Mouneyrac et al). Data loss in semiconductor memory can occur if the radiation can penetrate the memory packaging material, reach and knock out electrons from the impurity/defect sites that lay in the forbidden energy band gap of silicon. Theoretically, is this possible? Let us find out. When DDR SDRAM is exposed to sunlight, some part of it is diffusely reflected, while most of it, is absorbed into the memory.

Wessner, (2006) stated that “silicon MOSFETs has an important reliability problem and is caused by injection of electrons from the channel into the gate oxide. The energy barrier at the SiO₂: Si interface is 3.1eV”. The value of absorbed sunlight energy is approximately 4.13 eV. So if the sunlight can cross the plastic material and reached the MOSFET gate of the memory, this would knockout electrons from the SiO₂ dielectric found under the MOSFET gate (band gap 3.1 eV) creating electron-hole pairs due to Einstein's photoelectric effect shown in Figure 3.

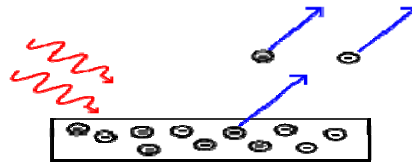


Figure 3: Einstein photoelectric effect.

The mathematical representation of photoelectric equation is:

$$hf = \Phi + K_{\max} \dots \quad (11)$$

The absorbed sunlight energy would cause polarization of electric charges in the BismaleimideTriazine (BT) plastic cover of the DIMM, because it has very high dielectric strength of 750V/mm, very high volume resistivity of 10^7 Mohm/cm³ and low dielectric constant of 4 at 1MHz EM radiation. The dielectric constant of BT at sunlight frequencies of 10^{12} to 10^{18} Hz is almost zero. Thus BT behave as a nonmagnetic material at these frequencies. Therefore the rate of decrease of magnetic component of transmitted EM in the BT is almost zero. In addition to polarization, the memory module would become warm due to its volume resistivity as evidence in

increase of temperature of CPU and mainboard components, recorded during data collection. The work function of BT, 5eV is greater than the energy possessed by the absorbed sunlight radiation, which is of about 4.13eV. Therefore sunlight radiation cannot liberate electric charges from BT molecules nor can it liberate electrons from the valence band of the silicon, because the radiation cannot cross the plastic cover of the memory module.

2.4 Different Types of Fault Defects in Semiconductor Devices

There are many different types of faults that developed in integrated circuits. Defects cause faults, errors, and failures in manufactured integrated circuits, and they yield loss and reliability degradation. Chughun, 2004 stated that “A fault is a critical defect which affects the performance or critical functional behaviour of integrated circuits. Defects can be classified into several types according to their size, sources, location and types. They are global and point defects, hard and soft defects, interlayer and intra layer defects, functional and parametric faults, permanent and temporary faults.

The CMOS is a promising technology used in fabricating semiconductor devices such as DDR memory, because it can be scaled down to smaller and smaller dimension which lead to higher MOSFET switching speed and integration density. As the size of CMOS is continuously scaled down, there are reliability concern associated with the scaling down of fabricated components in integrated circuits. According to Xiaobin, 2005, the Time-Dependent Dielectric Break down (TDDB) and hot-carrier induced degradation demonstrated that CMOS scaling would aggravate its built-in reliability.

1.1 Description of the Study Area

Kaduna state latitude $10^{\circ} 20'N$, longitude $7^{\circ} 45'E$ and Katsina state latitude $12^{\circ} 15'N$, longitude $7^{\circ} 30'E$ are located in the north west zone of Nigeria, is the case study area. It is endowed with rich sunlight and artificial sources of electromagnetic radiations such as mobile phone based transceivers, as well as the proliferation of radio/television transmitters in the area, and all these can cause data loss in computers. There are also abundance of ICT facilities such as internet café, desktop and laptop computers in the area, that are exposed to the above sources of electromagnetic radiations on daily basis, while they were put in use or while idle. The exposure of these technologies to radiation is most of the times due to human factor and or weather condition. For example, the constant exposure of computer system to incoming sunlight through a window that can reached the system if located at nearby window. This prolong exposure can cause data loss in computer systems or other related ICT facilities.

3. Research Method

For the purpose of carrying out this work, three number of DDRI and three number of DDRII were selected as samples using random sampling method based on their family data storage capacities(Mb), transfer data rates(Mbps), I/O widths, Burst lengths and Supply voltages (V). The selected samples were purchased from different computer

vendors in Katsina town. They were connected one per experiment to dual DIMM slots of Pentium IV 3059MHz desktop computer system that had windows XP, as operating system required to run the memory diagnostic software V3.1beta that was used in testing the samples. It was downloaded from CST corporation USA wave site into a CD-ROM. The CD containing the software was inserted in the CD-ROM drive of the above Pentium VI desktop computer. The system was powered and booted using the CD. After the software was loaded, it was configured to test the six samples for faults, with all its full test patterns activated. Each sample was first tested for faults inside a building before they were irradiated with sunlight, and second test was carried out on each sample during their irradiation with sunlight outside building, at six data collection centers, three in Kaduna state and three in Katsina state. A data logging meter model TES-1333R made by TES electronic corporation, Taiwan was used to measured the sunlight power densities that incidented the samples during exposure. A multimeter, made by MASTECH, USA was placed beside the experimental setup shown in Figure 5, to measured the temperatures and relative humidities of the environment under which the experiments were conducted. The results obtained were recorded in tables 3 to 6. Eighteen experiments were conducted in six locations in the months of of October, November, December, 2010 and January, 2011. In Kaduna state, Ikara latitude 11.18°N and longitude 8.23°E , Kaduna latitude 10.52°N and longitude 7.44°E , Kagarko latitude 9.45°N and longitude 7.68°E were selected as data collection centers, because they are having the maximum, medium and minimum yearly average daily solar constants in Kaduna state as shown in table 1, generated from RETScreen. While in Katsina state, Daura latitude 13.03°N and longitude 8.28°E , Katsina latitude 13.00°N and longitude 7.53°E , Funtua latitude 11.53°N and longitude 7.32°E were selected, because they are having the maximum, medium and minimum yearly average daily solar constants in Katsina state as shown in table 2.

Table 1: RETScreen, yearly average solar radiation for different locations of Kaduna state.

Locat.in case study area	Lat (o)	Long. (o)	Yearly aver. Daily solar rad.(KWh/m ² /d)	Earth temp. (oC)	R. Humid (%)
Ikara	11.18N	8.23E	5.87	27.1	50.0
Zaria	11.07N	7.70E	5.78	26.6	53.2
Kauru	10.65N	8.15E	5.69	25.9	56.4
Igabi	10.78N	7.77E	5.65	26.0	59.2
Kaduna	10.52N	7.44E	5.65	26.0	59.2
Saminaka	10.83N	7.90E	5.65	26.0	59.2
BirninGwari	10.67 N	6.55E	5.59	26.9	60.0
Kagarko	9.45N	7.68	5.45	26.0	64.7

Source: Generated from NASA Surface Meteorology and Solar Energy: RETScreen Data.

Table 2: RETScreen, yearly average solar data for different locations of Katsina state.

Locat. in case study area	Lat (o)	Long. (o)	Yearly aver. Daily solar rad.(KWh/m2/d)	Earth temp. (oC)	R. Humid (%)
Ikara	11.18N	8.23E	5.87	27.1	50.0
Zaria	11.07N	7.70E	5.78	26.6	53.2
Kauru	10.65N	8.15E	5.69	25.9	56.4
Igabi	10.78N	7.77E	5.65	26.0	59.2
Kaduna	10.52N	7.44E	5.65	26.0	59.2
Saminaka	10.83N	7.90E	5.65	26.0	59.2
BirninGwari	10.67 N	6.55E	5.59	26.9	60.0
Kagarko	9.45N	7.68	5.45	26.0	64.7

Source: Generated from NASA Surface Meteorology and Solar Energy: RETScreen Data.

3.1 Experimental Setup for Testng Fault in DDR Sdram Due to Sunlight Exposure

The mainframe of desktopcomputer was opened, and each sample (three DDRI and three DDRII) wasconnected to a DDRI DIMM slot or DDRII DIMM slot located on the motherboard of the computer. It has dual DIMM slots capable of accommodating of DDRI and DDRII SDRAM. Refer to Figure 4 on how to slot in either DDRI or DDRII in dual DIMM slots

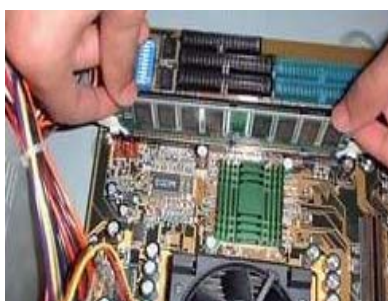


Figure 4: How to slot in DDRI or DDRII to be tested in PC mother board.

Then the desktop was inserted inside a wooden casing as shown in Figure 5 (the experimental setup). The casing wooden top cover was slightly raised up, this was how only the samples tested were exposed to sunlight radiation during experimentation. The LCD monitor, the keyboard, the UPS and the mouse were all connected at the I/O ports of the desktop top computer. The wooden casing was cut at the rear of the mainframe of the desktop computer, to provide access to the ports. The casing was inclined at an acute angle (depending on the sun horizon) to the ground, with the casing front face facing the sun, so that only the sample under test was exposed to maximum sunlight radiation. Data logging solar meter model TES1333R (made by

TES electrical electronic corporation, Taiwan) was used to measure the solar power densities that incidence the samples tested. This meter was attached at the top of the power supply unit of the mainframe

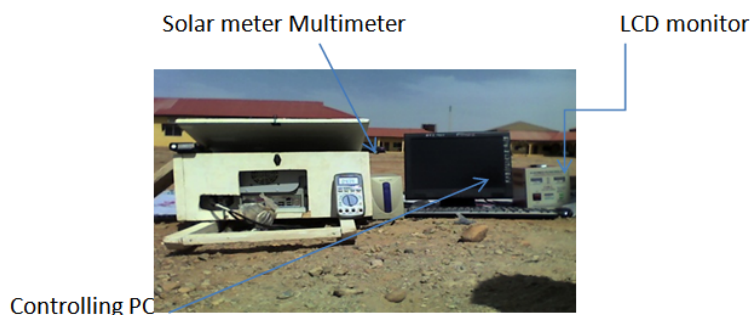


Figure 5: Experimental set up for testing data loss in DDRI or DDRII due to sunlight irradiation.

As shown in Figure 5, in such a way that it measured the sunlight radiation that fell perpendicular on the plane surface of the sample under test. A solar meter was attached to the wooden casing in such a way that its front surface was parallel to the bottom cover of the PC mainframe and perpendicular to the plane of DDRI or DDRII under test, in order to obtained accurate measurement from the meter. Another meter(multimeter) model MASTECH 8209 made by MASTECH, USA, was attached beside the casing and it measured the atmospheric temperature and relative humidity of the environment under which the different tests were conducted.

3.2 Measurement of Data Loss in DDR Sdram Samlpes Due to Sunlight Irradiation

In this work, six hour measurements per day were conducted for eighteen days, that studied the effect of sunlight radiation on data stored in three DDRI and three DDRII samples. For data loss measurement, the computer was booted from the CD-ROM drive that contained diagnostic software. After it was loaded by the PC, it was configured with all its test patterns fully activated. .In other words it was configure to run on walk data "0"& "1", walk address "0"&"1", mats+, march B, march C, checkerboard and bust test patterns. According to CST Corporation, 2011, these are the test patters that semiconductor industry recognizes as excellent chooses for uncovering assembly error and memory cells failure. The first test on each sample was carried out faults inside a building, where they were not exposed to sunlight radiation and it covered the base and extended memory address locations. While the experiments were conducted inside the building, the sunlight power densities, the atmospheric temperature and relative humidity inside the building were measured using solar meter model TES 1333R and multimeter model MOSTEC 8209, on half hour basis, for six hours per day per experiment. Then, experimental setup was brought out of the

building, and the samples were similarly tested for faults outside building, where they were exposed to sunlight radiation. The samples tested outside building, were made to received maximum sunlight by occasionally changing the inclination and the orientation of the experimental set up towards the sun.

4. Results Obtained

The data obtained are recorded in tables 3, 4, 5 and 6. Table 3 shows the result obtained for memory diagnostic tests carried on six samples, outside a building (where the samples were not exposed to sunlight radiation), at an average temperature of 34.4°C and 53.7 %RH. The table shows that the memory diagnostic software V3.1 beta detected faults from 192Mb to 256Mb memory address locations of the 256Mb DDRI333. This is 25.0 % of the total data storage capacity of this sample. The same table shows that the 256Mb DDRI200 and 256Mb DDRII200 have memory address fault locations from 191Mb to 256 Mb memory space. This is 25.4 % of the data storage capacity of each of them. Also the V3.1 beta diagnostic software detected faults in 512Mb DDRI 266 and in 512Mb DDRII667 from 447Mb to 512Mb memory space. This is 12.7% of the data storage capacity of each of the two memory modules, and this is shown in table3. While the faults detected in the 1024Mb DDRII667H memory sample is from 959 Mb to 1024Mb, and this 6.3% of its data storage capacity. The faults in the six samples were picked by six out of the ten test patterns activated, while running the diagnostic software V3-1 beta. Thus are: walk address '0', mats+, march B, march C-, checker board test patters.

Table 3: Experimental result obtained on three number of DDR1 and three number of DDRII before their irradiation with sunlight.

Measurand	No. of six hour experiments carried out. 1 1 1 1 1 1						Aver
Aver atm. temp. oC	33.8	34.8	34.7	32.7	35.4	35.2	34.4
Aver relat. humid. %RH	53.7	50.8	29.5	40.4	47.3	24.5	41.0
Aver solar power dens Io W/m2	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Type of DDR SDRAM	DDRI 200	DDRI 333	DDRI 266	DDRII 200	DDR II 667	DDRII 667H	NA
DDR SDRAM storage capacity(Mb)	256	256	512	256	512	1024	NA
Faulty addr. Detect. Mb)	191	192	447	191	447	959	404.5

Test patterns that pick fault(s)	Walk address'0', Mats+, March B, March C-, Checker board, Burst						NA
% of faulty mem address	25.4	25.0	12.7	25.4	12.7	6.3	17.9

Table 4: Experimental result obtained during irradiation of three DDR1with sunlight.

Measurand	No. of six hour experiments carried out 1 1 1 1 1 1						Aver
Aver atm. temp. oC	36.3	35.9	34.8	36.0	37.9	35.6	36.1
Aver relat. humid. %RH	21.2	43.0	29.8	16.2	15.9	12.8	23.2
Aver solar power dens Io W/m2	631.4	557.6	635.7	477.2	711.5	493.2	584.4
Type of DDRSDRAM	DDRI 200	DDRI 333	DDRI 333	DDRI 266	DDRI 266	DDRI 266	NA
DDRSDRAM stor.capac(Mb)	256	256	256	512	512	512	NA
Faulty Addr detected(Mb)	191	192	192	447	447	447	319.3
Test patterns that pick Fault(s)	Walk address'0', Mats+, March B, March C-, Checker board, Burst						NA
% of faulty mem. address	25.4	25.0	25.0	12.7	12.7	12.7	18.9

The result obtained during the exposure of the samples to sunlight in the months of October, November, December, 2010 and January, 2011 are shown in Tables 4, and table 5 found next page. Comparing the result in table 3(before irradiation of the samples) with the results in tables 4 and 5 (during irradiation of the same samples with sunlight), it can be seen that the irradiation of the samples did not lead to recording of additional faulty memory location which differ from the ones recorded in table 3, during the testing of the samples before their irradiation with sunlight. Tables 4 and 5 indicated that the 256Mb DDRI 200/PC2-4200U444-2 and 256Mb DDRII 200/PC2-4200U-444-12 samples have faulty memory address locations from 191Mb to 256Mb of their memory space, and this is 25.4 % of each data storage capacity. The faults were detected by the software model V3.1 beta at 36.3°C, 32.7°C average temperatures and 21.2%, 40.4% average relative humidities respectively. The result for 256Mb DDRI333/ DNKMBU256BTE sample is in table 4, and it has faults from 192Mb to 256Mb memory space, and this is equivalent to 25.0% of its data storage capacity, at 35.9°C, 43.0%RH. The same result was obtained (table 3) before irradiation of 256Mb DDRI333/ DNKMBU256BTE with sunlight.

Table 5: Experimental result obtained during irradiation of three DDRII with sunlight.

Measurand 1	No. of six hour experiments carried out 1 1 1 1 1 1						Aver
Aver atm.temp. oC	35.1	34.9	27.4	33.1	36.8	34.6	33.7
Aver relet. Humid. %RH	40.4	34.9	29.5	12.3	13.6	37.9	28.1
Aver solar power dens Io W/m2	763.1	840.5	384.9	637.7	744.7	803.1	695.7
Type of DDRSDRAM	DDRII 200	DDRII 200	DDRII 667	DDRII 667	DDRII 667H	DDRII 667H	NA
DDRSDRAM stor.capac (Mb)	256	256	512	512	1024	1024	NA
Faulty Addr detected(Mb)	191	191	447	447	959	959	532.3
Test patterns that pick Fault(s)	Walk address '0', Mats+, March B, March C-, Checker board, Burst						NA
% of faulty mem. Addr.	25.4	25.4	12.7	12.7	6.3	6.3	17.9

Tables 4 and 5 show that the 512Mb DDRI 266/KVR266x64C25 and 512Mb DDRII 667/KVR667x64C3A have the same faulty address locations detected by the software, that is from 447Mb to 512Mb of each memory space, and this is equivalent to 12.7 % of each memory data storage capacity. They were tested at 35.4°C and 47.3%RH average temperature and relative humidity. The same result was obtained (in table 3) before the two samples were exposed to sunlight radiation.

The result obtained from testing the 1024Mb DDRII 667H/PC(table 5), shows that the module has faulty memory address locations from 959Mb to 1024Mb, translating to 6.3 % of the memory module data storage capacity, at 35.2°C, 24.5%RH.

4.1 Discussion of Result

The test carried out on the six samples before and during their irradiation with sunlight, were found to have faulty memory address locations as indicate in tables 3,4 and 5. The faults were picked up by walk address '0', mats+, march B, march C-, checker board and burst test patterns of the diagnostic software model V1.45 loaded and run from CD-ROM drive of the desktop computer. The results from tables 3-5 show that the faulty address locations detected by the software are not residing in the base memory address location (from 0-1Mb) of the sample tested. This memory space is where the operating system of a computer is loaded when it finished booting. Since there were no faults in the base memory area of the samples tested, so there were no faults detected by the BIOS when ever the computer was energized from the a.c. mains, regardless of the presence of the faults detected by the diagnostic software in the extended memory area of the six DDR SDRAMs tested. Table 5 shows the result obtained for

DDRII/KVR667x64C3A/512MB when it was irradiated with sunlight and tested for six hours in Katsina data collection center and for another six hours in Funtua, a total of twelve hours test. This sample refused to boot the computer for carrying out subsequent test. The BIOS of the computer continued to give out continuous long beep sound which is an indication of memory hardware fault in the DDRII/KVR667x64C3A/512MB. Table 5 shows the result obtained for DDRII/PC2-4200U-444-12/256MB when it was irradiated with sunlight and tested for six hours in Kaduna data collection center and for another six hours in Birningwari, a total of twelve hours test. This sample also refused to boot the computer for carrying out subsequent test. The BIOS of the computer continued to give out continuous long beep sound which is an indication of memory hardware in the base memory address location of this sample. The beep sound is a standard method of indication of faulty memory connected to the DIMM slot of computer system. The fault detected by the BIOS shows that the DDRII/PC2-4200U-444-12/256MB had developed fault in its base memory area a day after it was irradiated with sunlight for twelve hours. Table 5 shows that this twelve hours test during sunlight irradiation occurred at an average power density of 801.8W/m^2 , 35.0°C average temperature and 37.7% average relative humidity. The DDRII/PC2-4200U-444-12/256MB was assembled by hynix in China. The second memory DDRII/KVR667x64 C3A/512MB slot of computer system. The fault detected by the BIOS shows that the DDRII/KVR667x64 C3A/512MB had developed fault in its base memory area a day after it was irradiated with sunlight for twelve hours. Table 5 shows that this twelve hours test during sunlight irradiation occurred at an average power density of 511.3W/m^2 , 30.3°C average temperature and 20.9% average relative humidity. The DDRII/KVR667x64 C3A/512MB was assembled by Kingston in Taiwan.

Schroeder, Pinheiro and Weber, 2011 reported that, for normal operating environmental conditions, 94% of computer platforms have 20% of their correctable errors emanated from DRAMs.

Tables 3, 4 and 5 show that the amount of faulty memory spaces that is 64MB or 65MB of the upper memory area of the six samples are constant irrespective of irradiation of the samples. This implies that the faults in the six samples are not due to their exposure to sunlight radiation. They are fixed faults, rather than temporary faults, and were with the samples, right from place where they were purchased from the computer vendors. This work has not investigated the source of these faults. Radiation hardening wikipedia, n.d, stated that "The presence of residual radiation from radioactive isotopes in packaging materials of the memory modules is one of the major radiation damage sources to electronics.

Other sources are traces of radioactive elements in the materials used in their packaging, or production defects introduced at factory. Table 6 shows the % of total memory location address covered or done in the samples by the six test patterns, before they uncovered faults in the memories. The % are indications on how deep the six test patterns searched the memories before they uncovered the faults. Figure 5 also shows

the different test vectors patterns written in the memory adresslocations by the diagnostic software and the data it read back, before it detected faults in the samples.

Table 6: Experimental result obtained showing how deep the test vectors searched the six samples for fault and the type of faults detected.

Memory tested	% of address done by six test patterns before uncovering faults Walk addr. '0' Mats+ March B March C- Checker board Burst					
256 Mb DDRI200	71.4	37.5	18.8	15.0	37.5	21.8
256Mb DDRI 333	71.4	37.5	18.8	15.0	37.5	21.9
512Mb DDRI 266	69.0	43.7	21.9	17.5	43.7	23.3
256Mb DDRII200	71.4	37.5	18.8	15.0	37.5	21.9
512Mb DDRII667	69.0	43.7	21.9	17.5	43.7	23.4
1024Mb DDRII667 H	66.7	46.9	23.4	93.8	46.9	24.3
Written data pattern	Arbitrary	55AA55A A	33CC33C C	66996699	33CC33C C	00000000 0
Read back data	Change in data	FFFFFFFF	FFFFFFFF F	FFFFFFFF F	FFFFFFFF F	FFFFFFFF F
Type of fault detected	Addr. Bit-err:07FFFF C	Stuck at fault	Stuck at faults	Stuck at faults	Short b/w adj. colum& data lines	Burst functional failure

The above table shows that the DDRI and DDRII tested, have the same data storage capacities, and also have the same % of faulty address locations uncovered by the test patters walk address'0', mats+, march B, march C-, checker board and burst. The memory diagnostic software v i.45a had detected multiple faults in the six samples, that is short between adjacent columns and data lines, address bit errors, stuck at faults and burst functionality failure. The result in table 8 shows that as the data storage capacities of the six samples increase from 256Mb to 1024Mb, so do the % of faulty address locations detected by mats+, march B, march C-, checker board and burst test patterns. One of the character of the faults detected in this work is that, as the data storage capacities of the samples decrease from 1024Mb, 512Mb, 256Mb, so do the % of address location covered by walk address '0' test pattern done before this test

vector detected faults, increases from 66.7% to 71.4% and this is shown in table 6. Another characteristic of the faults detected is shown in bar chart in Figure 6 found next page . It shows that the increase in the memory speeds of the six samples do not have any effect on the % of address locations covered by the test patterns before they detected faults in the samples.

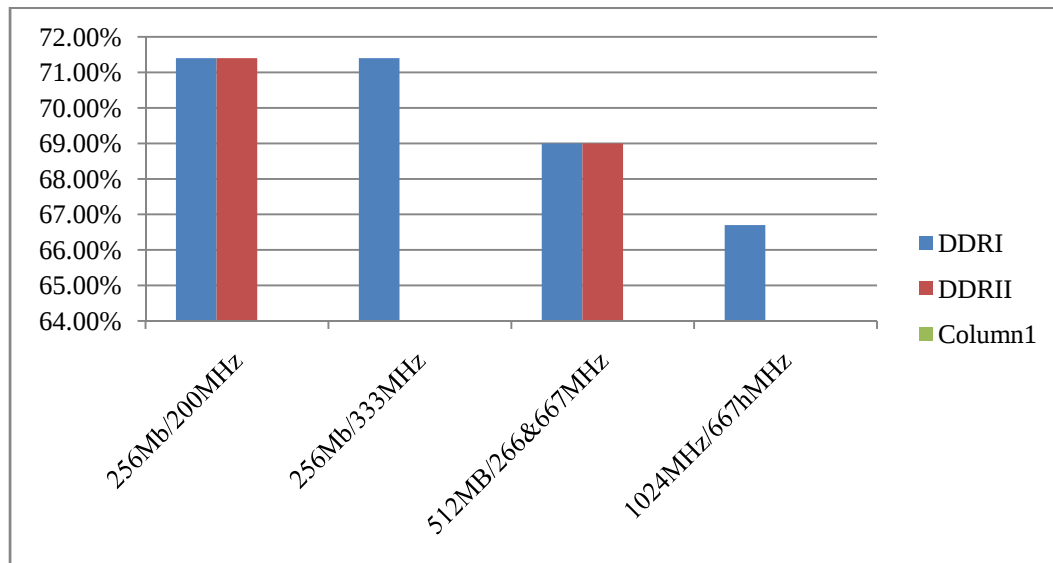


Figure 6a: % of address covered by walkaddr. '0'

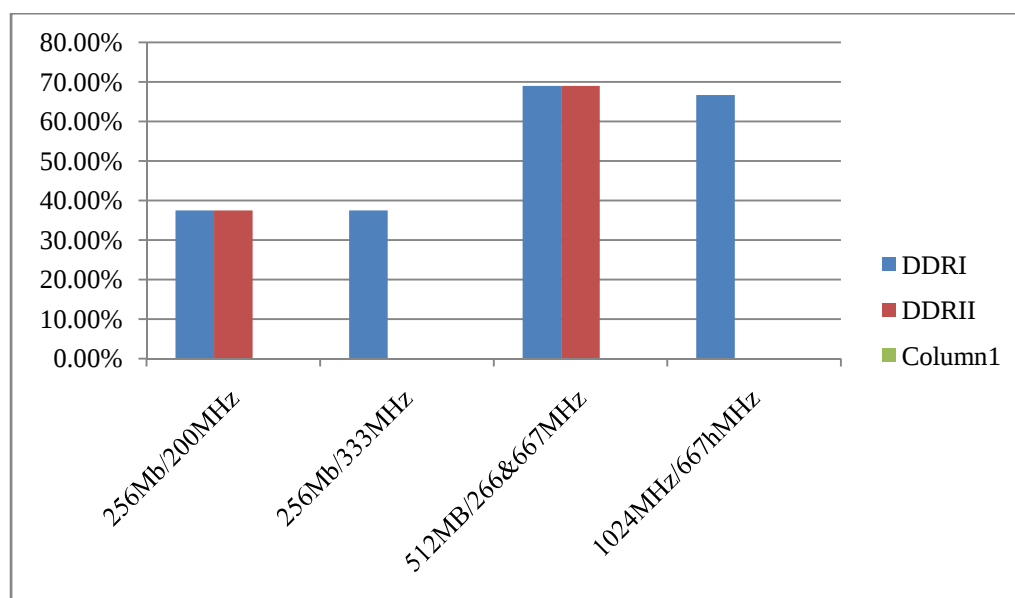


Figure 6b: % of address covered by mats+

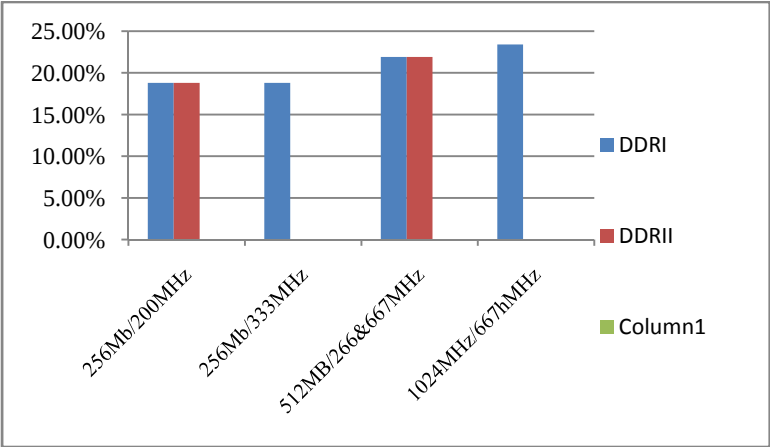


Figure 6c: % of address covered.

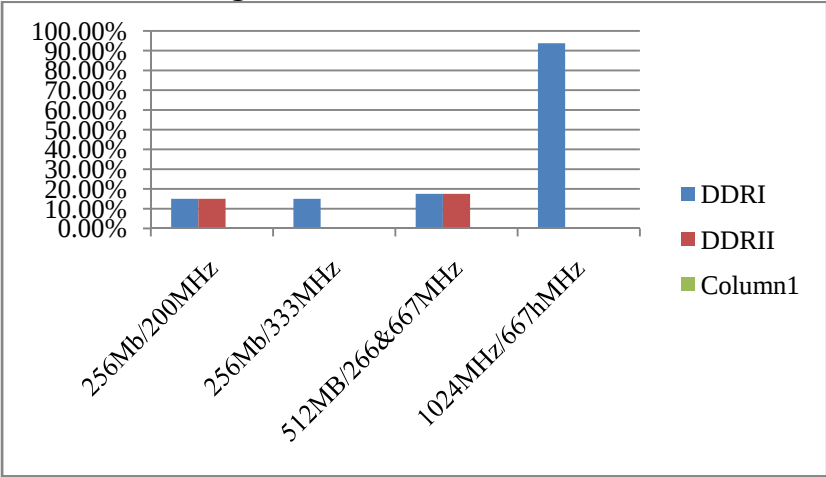


Figure 6d. % of address covered by march C- by march B.

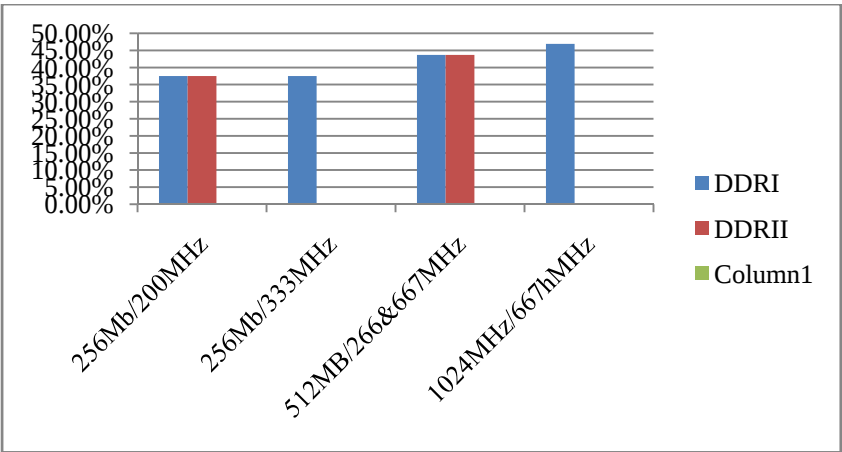


Figure 6e: % of address covered.

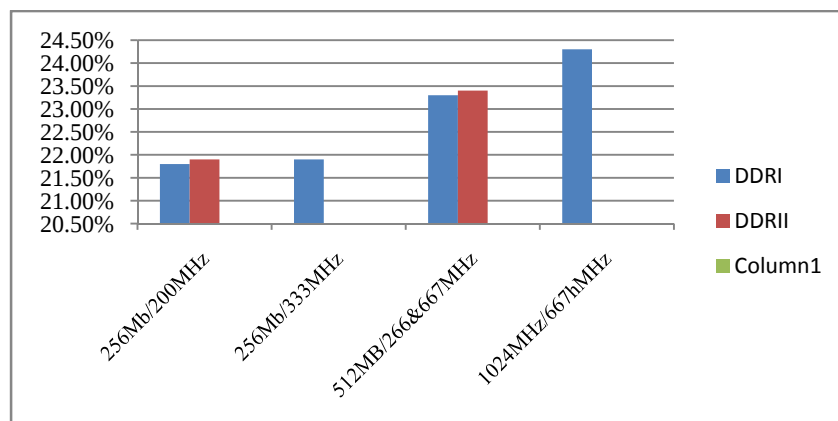


Figure 6f: % of address covered by burst by checker board.

5. Conclusion

This work has investigated the effect of solar radiation on data stored in three solar radiated DDRI samples and three solar radiated DDRII memory samples. Below are itemized conclusion of this work.

- i) During the first test using diagnostic software version V1.45a, it detected the presence of residual faults viz; Stuck at fault, bit error fault, lack of burst functionality during read or write cycle, and short between adjacent columns and data buses of the memory cells.
- ii) The same faults were detected by the same software in the six samples during their exposure to sunlight radiation.
- iii) It was discovered that, either the 64Mb or 65Mb upper memory area of the six DDR SDRAM tested before and during their exposure to sunlight have residual faults and this area is 6.3% to 25.4% percentages of the data storage capacity of each sample tested.
- iv) This work has discovered that at the time of irradiation of the six memory samples with solar radiation, there was no data loss detected by the diagnostic software recorded in any of the samples. But a after twelve hours test of the samples had elapsed and on continuing of the subsequent tests, it was discovered that, DDRII/PC2-4200U-444-12/256MB and DDRII/KVR667x64 C3A/512MB samples refused to boot the computer for carrying out subsequent test. The BIOS of the computer continued to gave out continuous long beep sound which is an indication of memory hardware fault in the base memory address location of these samples.
- v) The four remaining samples which had not developed hardware fault were used for continuation of subsequent test, were irradiated with sunlight and tested for additional six hour without developing software or hardware faults as a result of the irradiation.

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