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Circuit Model for Interconnect Crosstalk Noise Estimation in High Speed Integrated Circuits

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Abstract

At today's speed requirements the passive and simple elements of a high speed design, the interconnects, PC boards, connectors and chip packages may contribute a significant part of the overall delay. These elements may cause glitches, resets, logic errors and other issues. As a result, signal integrity has become an increasingly significant problem in modern VLSI design. In order to deal with the challenges associated with crosstalk noise estimation and avoidance tools and technology should be included early to IC design cycle. Therefore during the signal integrity verification, noise width and peak noise values on sensitive nodes should be confirmed which are below the recommended threshold levels, so that given routing solution will not lead to logic failures caused by coupled noise. Hence, an efficient and accurate crosstalk noise estimation is required to confirm signal integrity with in a limited design cycle time. The previously designed models have not considered the distributed nature of an RC network which is needed in Deep Sub Micron (DSM) designs. The coarse distributed RC characteristics of global interconnect to be considered to guide noise-aware layout optimizations. In this paper by considering the coarse distributed nature of interconnects the 8π circuit model is developed and the model is simulated using CADENCE and HSPICE. The average % error is within 6%. The model is also tested for different optimization techniques. The comparison of noise voltage for different driver sizing in 2π, 4π and 8π shows 8π is more accurate.

Keywords: Crosstalk; Interconnect; Modeling; Noise; Signal.

1. Introduction

In deep sub-micron (DSM) circuit designs, the coupling capacitance between adjacent nets has become a dominant component as taller and narrower wires are now placed closer to each other. The coupling capacitance not only leads to excessive signal delays but also causes potential logic malfunctions. The latter problem is especially serious for designs with higher clock frequencies, lower supply voltages and usage of dynamic logic since they have lower noise margin. To make sure a final layout to be noise immune, accurate and efficient noise models are needed to guide interconnect optimizations at various stages.

Several crosstalk models are developed to calculate crosstalk noise amplitude and crosstalk noise width. By simplifying the telegraph equations directly, [1, 2] deriving analytical equations for peak noise in capacitively coupled interconnects,using simple lumped circuit models, aggressor and victim net[3] by a simple L-type lumped circuit and obtained a bound for crosstalk noise using a step input, later extensions to this model to consider a saturated ramp input or π-type lumped RC circuit models are developed[4, 5, 6]. later proposed a 2-π model which affords better accuracy than previous models [7].By taking into consideration many key parameters, such as the aggressor slew at the coupling location, the coupling location at the victim net (near-inverter or near-receiver) and the coarse distributed RC characteristics for victim net.

This paper presents crosstalk circuit model for the noise constrained VLSI Interconnect optimization. The 8π circuit model is developed by considering coarse distribution RC characteristics for the victim net and coupling locations. The circuits are simulated using HSPICE. The applications of 8π circuit model for noise minimization techniques such as wire spacing and driver sizing are discussed. The paper divided into 5 sections, in section 2, the factors effecting the crosstalk is explained. In section 3 the developed circuit model is explained.In section 4 the results and the section 5 gives the conclusion.

2. Factors governing the Crosstalk level

2.1Wire Spacing

The magnitude of coupling capacitance between a victim net and its adjacent nets versus the victim net's capacitance to ground. The distance between two lines i.e aggressor and victim nets is d. The coupling capacitance between two lines is C_x , which is depending on the distance between the two lines. If the distance between two lines is low then the coupling capacitance will increase as shown in Figure.1, increasing the d will decreases the coupling capacitance value (ie $C_x/4$) as shown in the Figure.1. Therefore, the Coupling capacitance (C_x) is inversely proportional to the distance (d) between two nets. Ie $C_x \alpha \frac{1}{d}$

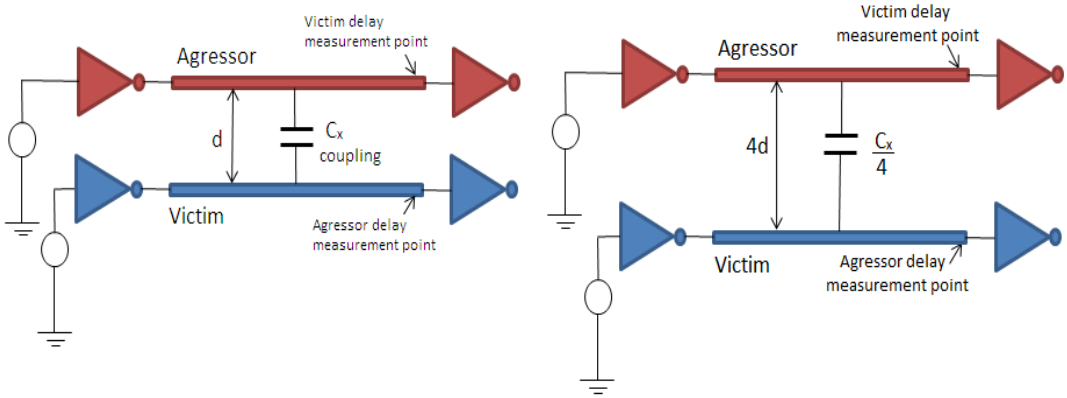

Figure 1: Aggressor and victim separated by a distance of 'd'.

2.2 Driver Sizing

Consider the driver in victim net which has driver resistance of 100Ω and 10Ω as shown Figure.2. If the driver resistance increases (100 Ω) then the size of the buffer decreases, lowering R_d (10 Ω) will involve increasing the bigger driver on the victim as shown in Figure.2. Bigger implies width/length ratio of its output transistors is a lot larger. The size of the driver is inversely proportional to the driver resistance.

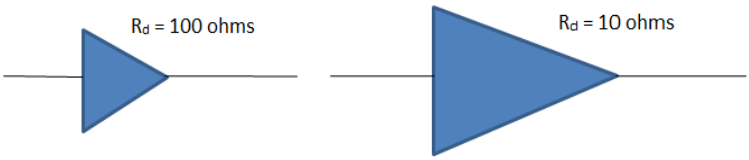

Figure 2: Driver size and resistance.

$$v_{\max} = \frac{(R_d + R_s)C_x}{t_r}\left(1 - e^{-t_r/t_v}\right)$$

From [7]

$\mathbf{v_{max}}$ is directly proportional to the driver resistance (R_d) and inversely proportional to the size of the buffer.

3. 8 π –Circuit Model

The 8 π model is extended to include the distributed RC characteristics of Interconnects. The multiline model is developed based on 2π model. The drivers are represented by linear resistance and other RC parameters are obtained based on the technology and geometric information. Here, the regions before coupling (L_s) and after coupling (L_e) are divided into four equal regions, which form 4π sections before the

coupling and 4π sections after the coupling location as in Figure.3, it forms 8π model which gives better accuracy compared to other two models are discussed in this section.

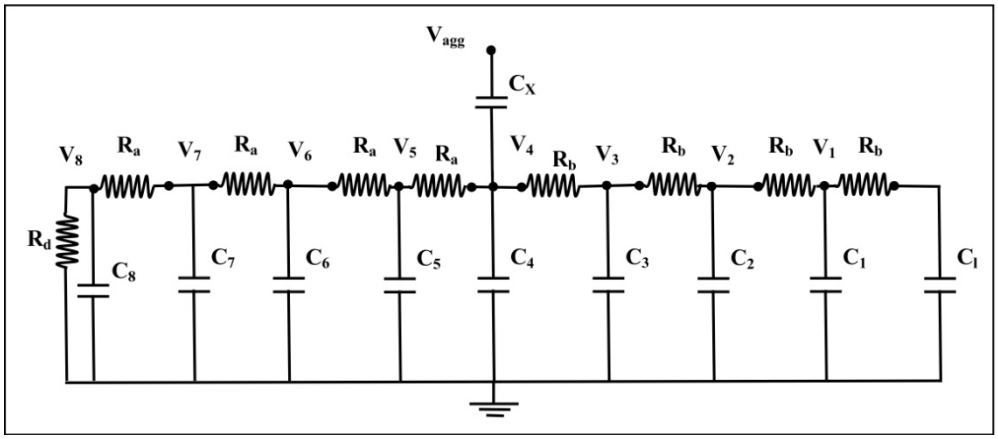

Figure 3: Simplified 8-π circuit model.

Writing node equations at different nodes for the circuit shown in Figure.3.The crosstalk noise is estimated and the circuit is simulated using CADENCE and HSPICE tools. The results are shown in section 4.

3. Results

The simulations are obtained for the optimum wire dimensions in 180 nm technology, with the driver resistance of 150 Ω and input 1v ramp and rise time t_r=50 ps.

Table 1: The comparison of noise voltage amplitude in 8π model for different Interconnect spacing.

S μm	Vp-Cadence	Vp-Hspice	%Error
0.1	0.7127	0.7	5.12649
0.2	0.51015	0.523	6.648217
0.3	0.4009	0.423	9.941407
0.4	0.3354	0.325	4.731861
0.5	0.27158	0.275	5.739853
0.6	0.2354	0.235	5.556747
0.7	0.2102	0.2	3.303268
0.8	0.1803	0.175	2.324778

From the Table.1 it is observed that the average % error is 5.421578%. The error is within 6%. Hence this model can be used for estimation of crosstalk noise.

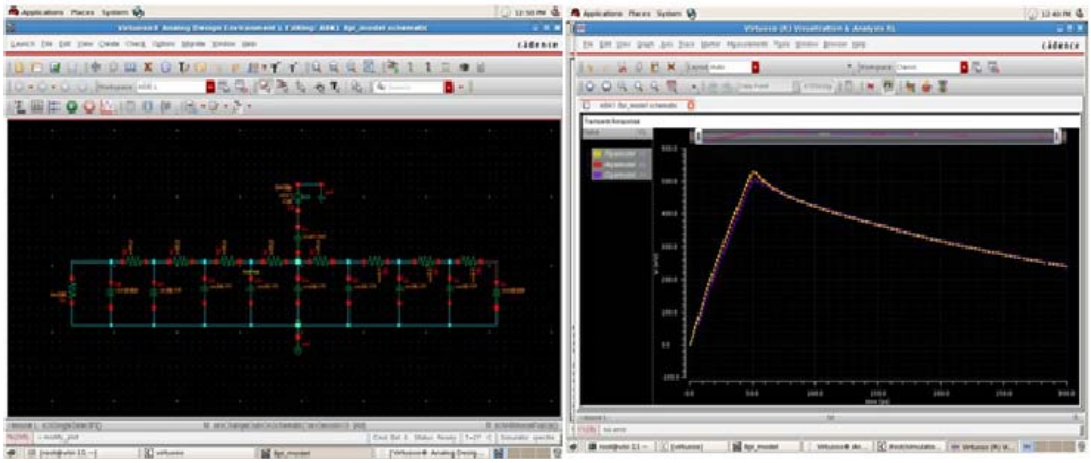

Fig. 5.77: 8 π Model circuit Schematic and Simulation output for 2π, 4π and 8π Models.

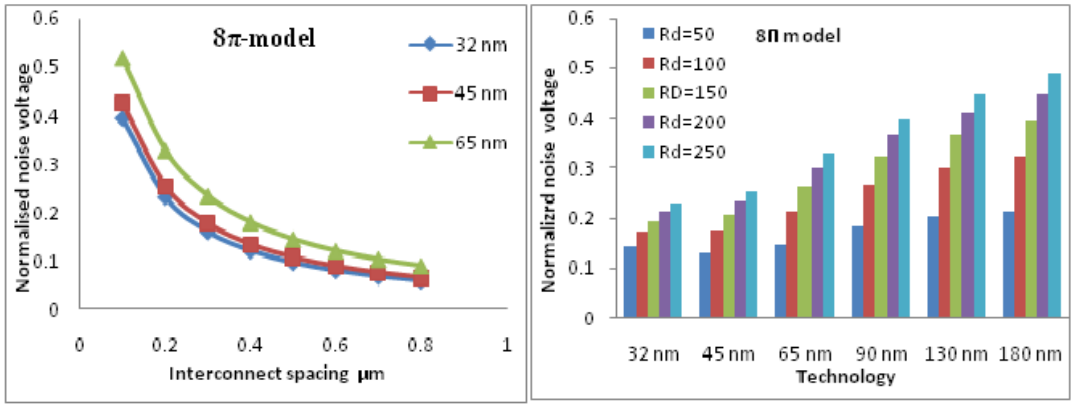

Figure: Effect of Interconnect spacing and Technology on crosstalk for 8π model and Comparision of noise voltage for different driver size and Technology.

4. Conclusion

The conclusions drawn from the results, while estimating noise in 8π model gives less than 6%, and it is observed that the 8π model gives better accuracy than 2π and 4π model while estimating the crosstalk noise amplitude and noise width. The developed circuit model is tested for different noise optimization techniques, such as wire spacing and driver sizing. It is also observed that driver sizing is more effective in noise minimization.

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