

On-chip Self Testing using BIST-oriented Random Access Memory

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Abstract

The increased circuit density in today's integrated circuits demands for efficient and low cost testing as compared to the testing of logic with external test equipment. The Built-In Self Test (BIST) architecture provides the self-testing of logic circuit but is not at the positive extreme in delivering deterministic and limited test vectors and storage and compression of output test responses. On-chip Self Testing using BIST-oriented Random Access memory employs a new logic BIST methodology that can deliver deterministic test vectors and stores the compacted of output responses in the memory. The circuit is tested with the predetermined test-vectors and the output responses are compacted and then compared with the original error-free values to detect the presence of faults, if any. The proposed scheme being presented in this paper consists of test data compression logic and on-chip SRAM structure, which acts as a ROM when the test mode is on. The new BIST oriented SRAM (BRAM) implements ROM features in the test mode and incurs no penalty in the normal SRAM mode of operation. BRAM can be designed by adding extra word line in a row to a SRAM cell. It stores the compressed test vectors that can be given to on-chip de-compressors during test mode. The de-compressor decompresses the compacted test data and gives to the CUT and the responses are compacted using a compactor circuit and this compacted response is compared with the original error free responses in a comparator circuit to detect the faults.

Keywords: Logic BIST, BRAM, compactor, de-compressor.

1. Introduction

Advances in the VLSI technology led to the higher performances and higher integration of circuit components in a single chip. But, the increased circuit density and components miniaturization has increased the test cost. To limit the test cost from increasing exponentially, several testing methodologies which can test the design off-chip and/or on-chip have been devised in the recent research works. The testing methodologies may be broadly categorized into 1) External Testing using Automatic Test Equipment (ATE) 2) Built-in Self Testing. The conventional ATE carries out testing process by generating the test vectors externally and then applying them to CUT. The cost, complexity and difficulty in interfacing of ATE increase with the increase in the complexity of VLSI circuits.

The alternative methodologies consist of test vector reduction [1, 3] and Built-In Self-Test (BIST) method. Built-in Self test is a technique it allows the design to check itself. The BIST architecture consists of pseudo random pattern generator (PRPG) [2] and output response analyzer (ORA). PRPG generates the test vectors required for the CUT. The PRPG works on the principle of random number generation using LFSR with initial predefined seed value. The Output response analyzer (ORA) compares the generated output with the actual output to detect the fault in the CUT. By using PRPG [4, 5] and ORA, BIST technology provides a large reduction in memory usage which results to the reduction in the test. BIST methodologies provide high fault coverage, thereby high yield at the cost of increased memory area in the chip for the storage of output responses and more complex interfacing facilities to the external automatic testing equipment. However, BIST technology cannot achieve the high fault coverage because of random resistance faults. To overcome these problems some methods are proposed but these methods leading to the bad impact on the delay and the area.

To reduce the test cost of the design, Researchers proposed test data reduction is the most efficient method. In this method, test vectors are compressed by using a compressor to decrease the storage memory. While applying the test vectors to the CUT these compressed test stimuli is given to the de-compressor which generates the large no. of test vectors, the ratio of decompression is determined by the capability of the de-compressor and extra bits present in the code. This paper presents the concept of self-testing using BIST-oriented RAM. The following section describes the proposed methodology, Section 3 describes the concept of BRAM, and the following sections consists of golomb coding, de-compressor, results and conclusion.

2. Proposed Methodology

The main concept of this paper is BRAM technology called on-chip self testing using BIST oriented random access memory. The proposed method stores the calculated test stimuli in the SRAM which acts as ROM in the test mode and BIST mode. The new technology BIST oriented random access memory acts as a ROM by inserting extra word line in the row of SRAM by deciding proper layout positioning which cannot decrease any performance of the RAM and it acts as SRAM in the normal mode of

operation. The BRAM continuously stores the reduced test responses from the circuit under test and also gives the reduced test data to the on-chip de-compressors. Due to this, the proposed method not only reduces the memory but also increases the fault coverage. The following paper consists of basic idea of the proposed method and the new memory structure and coding and decoding methods.

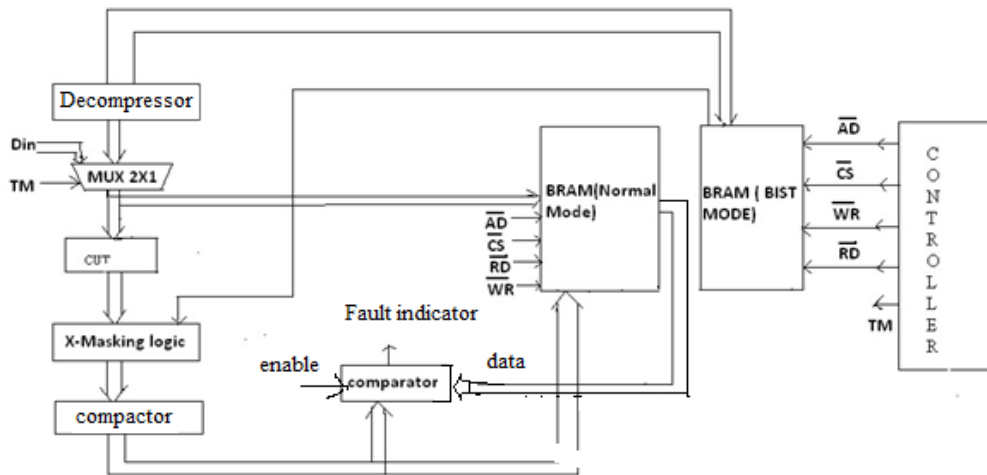


Fig. 1: On-chip self testing using BIST-oriented random access memory architecture.

The architecture consists of CUT, de-compressor, X-masking logic, compactor, BRAM and the FSM controller. In the normal mode $TE=0$, the BRAM acts as a normal SRAM which stores the output responses of the CUT. In the test mode or BIST mode $TE=1$, the BRAM gives the compacted test data to the on-chip de-compressor which decompresses into large no. of test vectors which given to the CUT. The responses from the CUT are given to the X-masking logic which masks the un-known values and sends the remaining values to the compactor which compacts or reduces the responses and given to the comparator which compares responses with the ideal values and detects the faults if any are present the CUT. The controller controls the whole operation and resets them after the whole operation is completed.

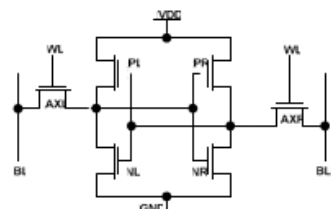


Fig. 2 SRAM cell

3. BIST Oriented SRAM Structure (BRAM)

The new proposed BIST oriented SRAM method, BIST oriented SRAM stores the compacted test stimuli in test mode and also act as normal SRAM in the normal mode i.e., test mode is off. SRAM can be converted into BRAM by adding extra word line in the row of the SRAM structure. The 6 transistor SRAM cell is shown in the above fig. The word line signal is shared by the two adjacent SRAM cells. So, the gate signals of all transistors are simultaneously turned off and on.

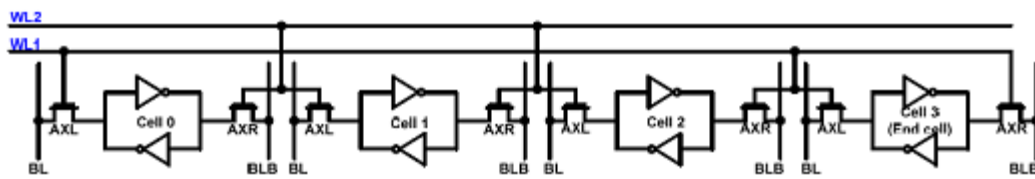


fig .3 schematic of BRAM cell

The main difference between SRAM and BRAM is that BRAM have 2 word lines which shown in the fig.3 the gate transistor is contacted with the any one of the word line. The operations of modes are described in the below.

A. Normal mode:

In this mode both the word lines (WL1 and WL2) are simultaneously switched off and on for write and read functions same as the normal SRAM operation.

B. BIST mode of operation:

In this test mode, read operation is done as the same way of SRAM but the writing test data in the BRAM is done in two using the two word lines

Step 1: When the WL1 and the WL2 are on, write 1's in all the bit cells (WL1=1, WL2=1, BL=1, BLB=0)

Step 2: when WL1 is off and WL2 is on, write 0's in all the bit cells (WL=0, WL=1, BL=0, BLB=1)

From the above fig, we can see that the transistors sizing weren't disturbed, only the access transistor gates AXL, AXR are connected to the word lines WL1, WL2 according to our test data. For storing 0 in the cell AXL is connected to WL2 and the AXR is connected to WL1 and also neighboring AXR. AXL, AXR which are present at ends of each row are connected together.

4. Golomb Coding and De-Compressor

The Golomb coding [9] is used to compress the test and also the test responses from the CUT. Golomb coding is based on the division algorithm method, the data is divided by the some constant no. M, we can select value of M depending upon the

compression range and width of the memory. The quotient of the division is taken as **q** and we coded the value with no. of 1's depends on the value and ends with a 0. Suppose the value of the q is 4 then the data is 11110. We can also use X-compaction algorithm instead of X-masking logic and compactor.

De-compressor [8] is used decompress the compacted test data to apply test vectors to the CUT. It consists of XOR gates and Flip-Flop's. It generates the test vectors by adding 0's are 1's in between the code word like LFSR. De-compression ratio depends on the compression ratio and no. of inputs of the CUT.

5. Simulation Results

The simulation results are shown in below figures.

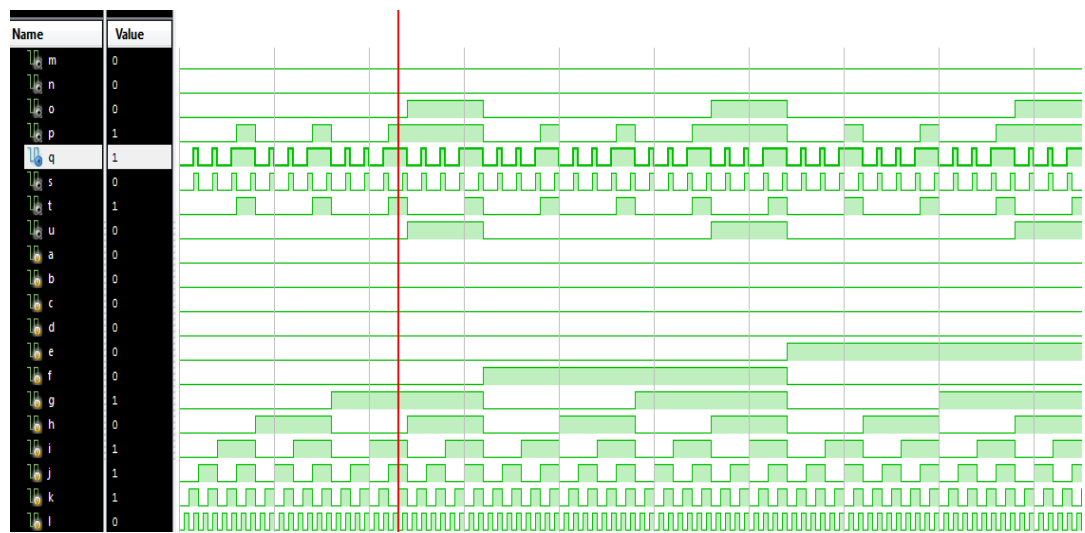


Figure 4: Simulation result of CUT

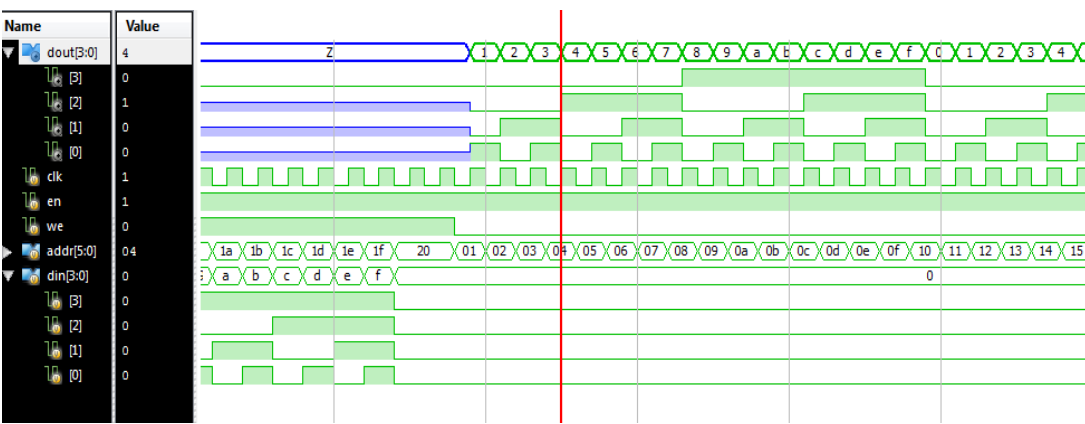


Figure 5: Simulation Result of BRAM

6. Conclusion

This paper presents a new testing methodology using new SRAM called BRAM which consists of test compression and de-compression logic and on-chip BRAM which can store and give the test data to the CUT. By using this methodology we can reduce the memory required for storing the test vectors and also there is no need of external ATE.

References

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