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Testability Design for Sleep Convention Logic

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Abstract

Memories of Flash are one more type of memory of non-volatile type on floating-gate transistors. The advantage of commodity and embedded flash memories will have rapid growth while we enter in the era of system-on-chip. Conventional tests for flash memory are usually ad hoc is the test procedure which is developed for a specific design. As there is a very large number of possible failure modes for flash memories. algorithms of long test that is automatic test equipment (ATE) which is complicated are usually seen. Production column and row address bit cell as basis to probe for any possible weaknesses of the process or design in SRAM. There occur faults sa0 and sa1 in any chip design, these faults will be overcome by using row, column address cells we make very perfect location to store the data or matter and cross sections of SRAMS will not occur. By the extend of cell check for memory array will verify the memory location for fault detection. The row address buffer and column address buffer will be used to pick the memory location. By comparing with previous method the above two modules gives accurate selection result for memory location for operation of cell checking.

I. INTRODUCTION

The main role of SRAM increased in System-on-Chip applications. Statistics shows that on average the total area of the chip exceeded from 50% by SRAM. In reported by us on the development of the smallest high-density 6T-SRAM cells for SOC using very good quality CMOS processes (3.87um2 for 0.18um technology node and 1.87 um2 for 0.13um technology node).And these cells are the most suitable in the applications of SOC to meet the high demand for high-density and high-performance and are vastly manufacturable.

To make sure their manufacture ability, robustness and reliability, the ordinary PCM which is (Process Control and Monitoring) structures of the quality test that aren't adequate to the monitor the process for high density SRAM, due to specific interactions in between the SRAM design and the process of the SRAM design. Ordinary PCMs are of generic nature and aimed at the supporting of the process module of the robustness of development characteristics and the generic design rules (rules that can use in any possible combination and design environment). Therefore, these all structure designs may not be always allowing us for testing the robustness of the chosen SRAM design rules of the environment of the specific SRAM array. For example, here the structure of conventional poly bridging is designed very well so that the robustness of minimum poly-to-to-poly spacing design rule should be proved for very long and parallel poly lines. This structure will may not be much suitable for providing the feedback of SRAM, so typically the poly layer SRAM features are more complex to understand in this system.

The bridging of metal used here will also be applied same, where pattern of the SRAM is more complex in the nature than that of a simple collection of the metal lines of parallel and spacing uniform. A conceptual changing in design and use of electrical test structures for SRAM-driven process for development will be thus further needed: for testing structures fir the need of the process-development driven here as well as driving of the product. The set of the structures and testing is used here for the development and the characterises the process need to be complemented with the suitable set of structures which will prove the robustness of high density of SRAM design and help quickly to be identified and the related yield issue to be correct process and to be design the SRAM during phase of development.

II. DESCRIPTIONS OF THE STRUCTURES OF THE TEST

The electrical parameters used to prove robustness of the SRAM designs which including Measurement of leakage current the bridging of inter-layer and intra-layer, Resistance will be measuring to find integrity of the connections, the SRAM transistor characterization for monitoring the possible deviations from targets and beta ratio and evaluation of static noise margin for the designing of SRAM's functional robustness.

The designed test structures must be very sensitive enough to allow the monitoring of both systematic occurrences' and random occurrences of any the possible weakness of the memory cell. We also needed here to characterize the transistors of SRAM in accuracy, static noise margins and the beta ratios within the SRAM array environment. Hence, in our chip testing of SRAM qualification, SRAM test structures will be having designed by us to ensure the SRAM cell robustness and SRAM device characterises.

To ensure the manufacture ability of SRAM cells, we have to design a series of test cells which are target based for SRAM cell. Each cell modification enables us to test one specific robustness requirement in SRAM cell. We use here these modified cells of SRAM to build the larger arrays (~10,000 to cells of 100,000) the SRAM cells will repeat just like an SRAM array. The parameter interest (resistance, leakage current,

etc.) is after that the entire array would be measured here. Hence, the statistical information is gathered from a very huge number of cells, hence the confidence level will be increased in the quality robustness for each individual design rule or design feature. The particular structures of array will helps us to determine any additional SRAM cell design modifications that will further improve its manufacturability, give the feedback on the sensitivity of chosen critical designing rules for the process variations and ultimately will be able to use quick tests of the proposed process impact modifications for the SRAM design.

Compared to traditional structure designs of PCM test, then this innovative concept has advantages as follows. Test structures are more oriented SRAM-cell, hence are dedicated to prove the robustness of cell design. The data is here collected from the true SRAM array environment; hence so, the captures process to design interactions, as is usually observed in the real products. Finally, here these structures will allow evaluation of all the cells of SRAM rules of specific design as it is used in the SRAM array environment. Another way is to determine the critical design robustness rules is by split design rather than split process. In this method we are applying a constant bias to a layer of critical and followed by study inter-layer and intra-layer effects. For example, the size of poly layer by 10% of its minimum feature size, and then study effects such as poly to poly bridging or contact to poly bridging, or monitoring of the overall impact on cell leakage as that of function of this bias. Typically, the same information could be collected by a split lot experiment at photo or etch. This method will however, enables us to study the robustness of the rule specific design over a massive amount of lots and to be allowed us for studying the additional margin of the design rule of choice when a process split will be applied. This operation of the biasing had been applied here by us on all critical layers, e.g. poly, contact and metal 1.

III. PROPOSED DESIGN

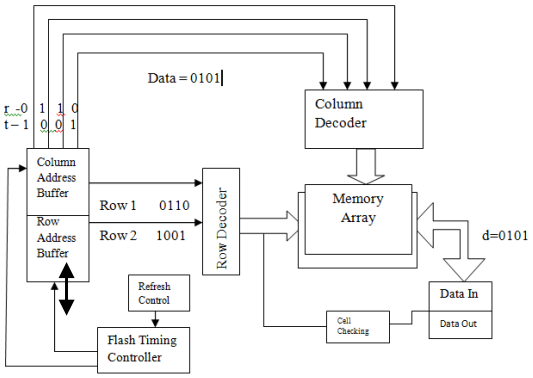

Fig 1. Proposed system

In the existing system there will be no cell checking operation so that it may be not verifying the memory location twice. There is only single memory cell array which is used to send the data in the single phase. There will be two problems in existing system, which are used to overcome these system problem we are here proposing a new architecture in this proposed system.

The proposed system consist of refresh controller, flash timing controller, column address buffer, row address buffer, column decoder, row decoder, memory array, cell checking, data in/data out these all are present in the proposed system.

The refresh controller and the flash controller will be refreshing all the data present in the memory array location. The row address buffer and column address buffer will be sending buffer of address now it may be column or row. The address buffer is took by their respective decoders which means column address buffer is given to the column decoder and the buffer of address is then decoded. Similarly in this way the row address buffer is given to the row decoder to decode the buffer of address.

The output of row and column decoder will be selecting the memory location in the memory array. As per the change of row address or column address buffer the decoder will be changing the location of memory. Then here the total memory location will call it as the memory array.

The block of cell checking will check either to select the memory location array i.e S=0 or 1. If S=0 the memory location array one of them will select, and the data is impend in that corresponding array memory location. Or Else S=1 the second array memory location will select and the data impend in second memory array location.

The date-in which is used for writing the data in array and data-out is used for reading the data in memory array. By using this proposed system we are going to overcome checking the memory array of two memory locations.

IV. RESULTS

The total output is shown below figure 2 as per the addresses of column and row data is stored in that given respective memory location

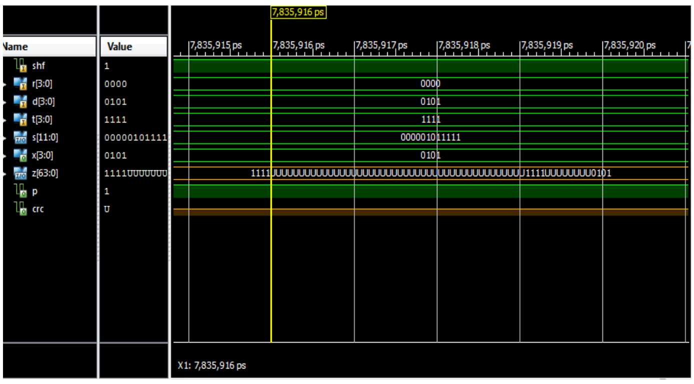

Fig 2. Technology Schematic

Here in this output we are giving inputs as u, v, w as 0,1 and the outputs are x, y. Then we are getting outputs same as inputs we give so that there is no fault if we get same output as input. And if the output is different from input then this indicate that there is fault in it so then we have to correct it. In this we get same output as input so that there is no fault in it.

V. CONCLUSION

As there is a large number of possible failure modes for flash memories, long test algorithms that is automatic test equipment that is called (ATE) it is complicated and they are commonly seen in this Production row address and column address bit cell as basis probe for any possible weaknesses of process or design for SRAM. There may occur sa0 and sa1 faults in any of these chip design, these faults overcome in order by using row address and column address cells and then we make perfect location for storing the data and there is no cross sections for SRAMS. By the extend of cell checking for memory array gives us the verification of memory location. The column and row address buffers are used for picking of the memory location. By comparing it with the previous method in the above two modules which gives accurate selection of memory location cell checking operation.

REFERENCES

[1] Ting-Jung Lin, Wei Zhang, and Niraj K. Jha, "SRAM-BasedNATURE: A Dynamically Reconfigurable FPGA Based on 10T Low-Power SRAMs" IEEE Trans. VLSI Systems, accepted for future inclusionin IEEE journal.

[2] I. Kuon and J. Rose, "Measuring the gap between FPGAs and ASICs,"*IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 26, no.2, pp. 203–215, Feb. 2007.

[3] W. Zhang, N. K. Jha, and L. Shang, "A hybrid nano/CMOSdynamically reconfigurable system—Part I: Architecture," *ACM J.Emerg. Technol. Comput. Syst.*, vol. 5, no. 4, pp. 16.1–16.30, Nov. 2009.

[4] A. DeHon, "Dynamically programmable gate arrays: A step towardincreased computational density," in *Proc. Canadian Wkshp. Field-Program. Devices*, 1996, pp. 47–54.

[5] H. Noguchi, Y. Iguchi, H. Fujiwara, Y. Morita, K. Nii, H. Kawaguchi,and M. Yoshimoto, "A 10T non-precharge two-port SRAM for 74%power reduction in video processing," in *Proc. IEEE Comput. Soc.Annu. Symp. VLSI*, 2007, pp. 107–112.

[6] Md. A. Khan, N. Miyamoto, R. Pantonial, K. Kotani, S. Sugawa, andT. Ohmi, "Improving multi-context execution speed on DRFPGAs," in*Proc. IEEE Asian Solid-State Circuits Conf.*, 2006, pp. 275–278.

[7] S. Trimberger, D. Carberry, A. Johnson, and J. Wong, "A

timemultiplexedFPGA," in *Proc. IEEE Symp.FPGAs for Custom Comput.Mach.*, 1997, pp. 22–28.

[8] T. Fujii, K.-I.Furuta, M. Motomura, M. Nomura, M. Mizuno, K.-I.Anjo, K.Wakabayashi, Y. Hirota, Y.-E.Nakazawa, H. Ito, and M.Yamashina, "A dynamically reconfigurable logic engine with amulticontext/multi-mode unified-cell architecture," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1999, pp. 364–365.

[9] Sapna Singh, NehaArora, MeenakshiSuthar and Neha Gupta(2012)"Performance Evaluation Of Different Sram Cell Structures AtDifferent Technologies", Proc. of International Journal of VLSI design &Communication Systems (VLSICS) Vol.3.

[10] W. Zhang, L. Shang, and N. K. Jha, "A hybrid nano/CMOSdynamically reconfigurable system—Part II: Design optimization flow,"*ACM J. Emerg. Technol. Comput. Syst.*, vol. 5, no. 3, pp. 13.1–13.31,Aug. 2009.

[11] G. Lemieux and D. Lewis, "Circuit design of routing switches," in*Proc. Int. Symp. FPGA*, 2002, pp. 19–28.

[12] Dr.Sanjay Sharma and ShyamAkashe (2011),"High Density Four-Transistor SRAM Cell With Low Power Consumption*", Proc. of Int. J.Comp. Tech. Appl*., Vol 2, 1275-1282.