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Design of Low Power and Area Efficient 64 Bits Shift Register Using Pulsed Latches

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Abstract

In low-power digital design, especially in shift registers, flip-flops (FF) plays a significant role. In move enrolls, the power utilization of framework clock is assessed to be half of the general framework control. This paper proposes a low-power and territory proficient move enlist utilizing computerized beat locks. The region and power utilization are lessened by supplanting flip-flops with beat hooks. This technique takes care of the planning issue between beat locks using various non-cover deferred beat clock motions rather than the ordinary single beat clock flag. A 256-piece move enroll utilizing beat hooks was created utilizing a 0.18μm CMOS process with VDD = 1.8V. The proposed move enroll spares 37% region and 44% power contrasted with the traditional move enlist with flip-flops. In advanced circuits, a move enroll is a course of flip lemon, having a similar clock, in which the yield of each flip-tumble is associated with the "information" contribution of the following flip-slump in the chain, bringing about a circuit that movements by one position the "bit exhibit" put away in it, moving in the information show at its information and moving out the last piece in the cluster, at each progress of the clock input. All the more by and large, a move enroll might be multidimensional, to such an extent that its "information in" and organize yields are themselves bit exhibits: this is executed basically by running a few move registers of a similar piece length in parallel.

Keywords: Area-efficient, flip-flop, pulsed clock, pulsed latch, shift register

I. INTRODUCTION

Flip flops are the fundamental stockpiling components utilized broadly in a wide range of advanced plans. As the element size of CMOS innovation process downsized by Moore's Law, planners can coordinate many quantities of transistors onto a similar bite the dust. The more transistors there will be additionally exchanging and more power scattered as warmth or radiation. Warmth is one of the marvel bundling challenges in this age; it is one of the primary difficulties of low power plan procedures and practices. The expanding essentialness of convenient frameworks and the need to confine control utilization (and henceforth, warm dispersal) in high thickness Very Large Scale Integration (VLSI) chips have prompted fast and inventive improvements in low-control plan amid the current years. Flip-flops (FFs) are the fundamental stockpiling components utilized broadly in a wide range of computerized plans. Specifically, advanced plans these days frequently receive serious pipelining systems and utilize numerous FF-rich modules, for example, enroll record, move enlist, and first in first out. It is additionally assessed that the power utilization of the clock framework, which comprises of clock conveyance systems and capacity components, is as high as half of the aggregate framework control. FFs consequently contribute a huge segment of the chip territory and power utilization to the general framework plan. Another driver of low power look into is the dependability of the coordinated circuit. Additional exchanging infers higher normal current is ousted and thusly the likelihood of unwavering quality issues happening rises. We are moving from portable PCs to tablets and considerably littler figuring computerized frameworks. With this significant pattern proceeding and without a match slanting in battery future, the all the more low power issues should be tended to. The present patterns will in the end order low power plan computerization on an expansive scale to coordinate the patterns of energy utilization of the present and future incorporated chips. Power] utilization of Very Large Scale Integrated outline is given by

II. SHIFT REGISTERS

A move enroll is the fundamental building obstruct in a VLSI circuit. Move registers are normally utilized as a part of numerous applications, for example, computerized channels, correspondence beneficiaries and picture preparing ICs Recently, as the extent of the picture information keeps on expanding because of the popularity for amazing picture information, the word length of the shifter enroll increments to process huge picture information in picture handling ICs. A picture extraction and vector era VLSI chip utilizes a 4K-bit move enlist A 10-bit 208 channel yield LCD segment driver IC utilizes a 2K-bit move enlist A 16-megapixel CMOS picture sensor utilizes a 45K-piece move enroll.

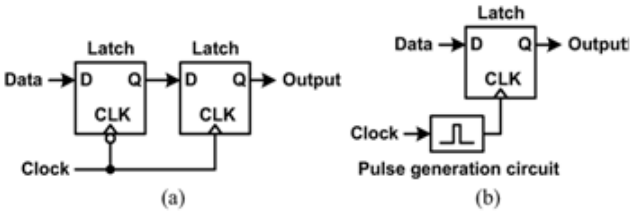


Figure 1: (a) Master-slave flip-flop. (b) Pulsed latch**.**

This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Shift registers can have both parallel and serial inputs and outputs.

III. PROPOSED ARCHITECTURE

A master-slave flip-flop using two latches in Fig.1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b). All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption 4-bitsub shifter register consists of five latches and it performs shift operations with five non overlap delayed pulsed clock signals (CLK_pulse<1:4>and CLK_pulse<T>). In the 4-bit sub shift register #1, four latches store 4- bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Fig. 4(b) shows the operation waveforms in the proposed shift register.

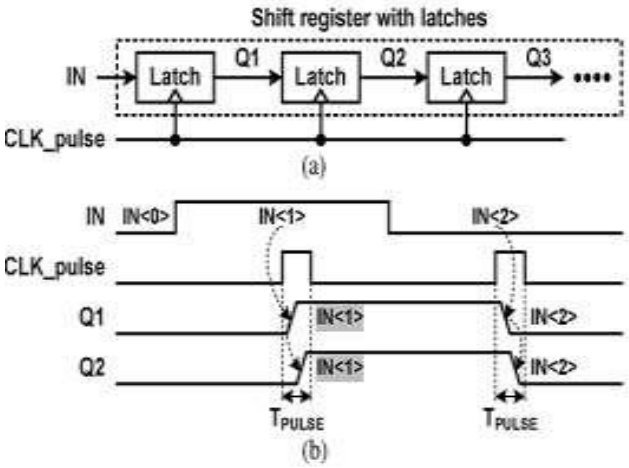
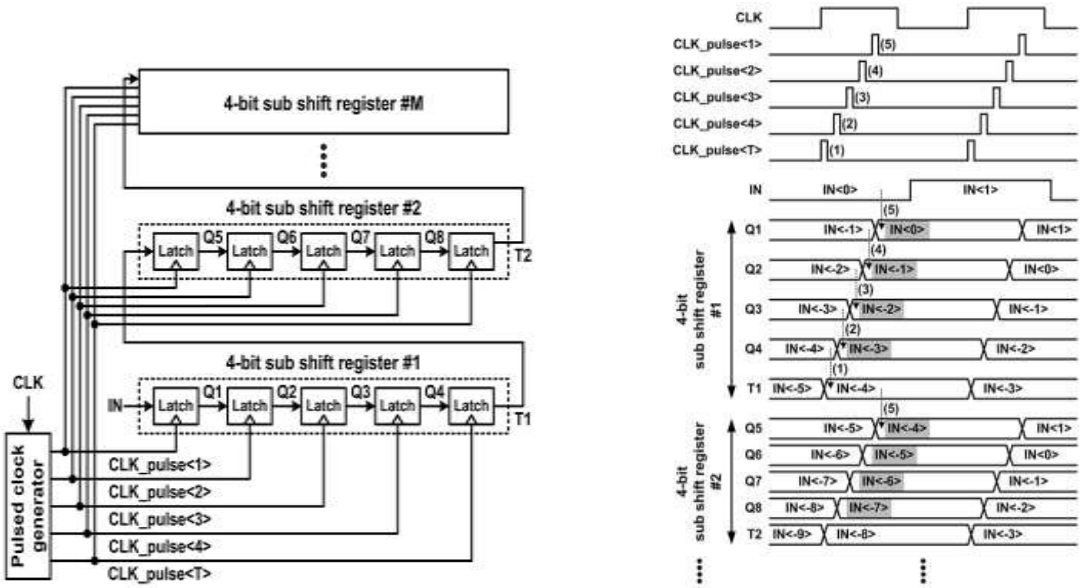


Fig. 2. Shift register with latches and a pulsed clock signal. (a) Schematic. (b)Waveforms



(a) (b)

Fig. 4. Proposed shift register. (a) Schematic. (b)Waveforms.

The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register is selected by considering the area, power consumption, speed.

Area Optimization: The area optimization can be performed as follows. When the circuit areas are normalized with a latch, the areas of a latchand a clock-pulse circuit are 1 and respectively, the total area becomes $\alpha_A \times (K+1)+N\left(1+\frac{1}{K}\right)$. The optimal $\mathrm{K}\left(=\sqrt{N/\alpha_A}\right)$ for the minimum area is obtained from the first-order differential equation of the total area $0=(\alpha_A - N/K)$. An integer for the minimum area is selected as a divisor of, which is nearest to $\sqrt{N/\alpha_A}$.

Power optimization: The power optimization is similar to the area optimization. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock-pulse circuit are 1 and, respectively. The total power consumption is also $\alpha_p \times (K+1)+N\left(1+\frac{1}{K}\right)$.

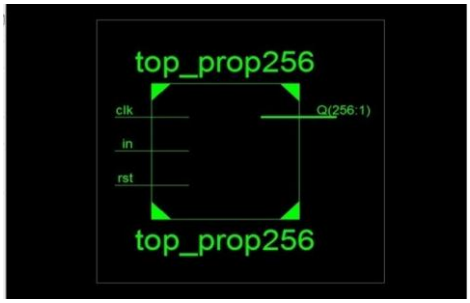
An integer for the minimum power is selected as a divisor of, which is nearest to $\sqrt{N/\alpha_p}$.

Chip Implementation: The most extreme check recurrence in the regular move enrolls is constrained to just the deferral of flip-flops in light of the fact that there is no postponement between flip-flips. In this manner, the territory and power utilization are more vital than the speed for choosing the flip-flounder. The proposed move enroll utilizes hooks rather than flipflops to decrease the region and power utilization.

V. SIMULATION RESULTS

Top Module:

RTL Schematic:



Design Summary:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	186	4656	3%
Number of Slice Flip Flops	322	9312	3%
Number of 4 input LUTs	5	9312	0%
Number of bonded IOBs	259	66	392%
Number of GCLKs	6	24	25%

Timing Report:

```
Data Path: m65/m1/Q_1 to Q<253>
                              Gate     Net
  Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name
  ----------------------------------------  ------------
   FDR:C->Q             1   0.514    0.357  m65/m1/Q_1 (m65/m1/Q_1
   OBUF:I->O                3.169           Q_253_OBUF (Q<253>)
  ----------------------------------------
  Total                     4.040ns (3.683ns logic, 0.357ns route
                                    (91.2% logic, 8.8% route)
```

CONCLUSION

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by substituting flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals as an alternative of a single pulsed clock signal.

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